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ELECTRICAL CHARACTERIZATION OF SIGNAL PROCESSING MICROCIRCUIT

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This report covers the work performed by the Reliability Assurance Branch of the Rome Air Development Center pertaining to the electrical characterization and MIL-M-38510 specification of analog microcircuits. The report is divided into sections covering specific device types, test methodology, electrical characterization data and results. The following device types/families were characterized with their respective military specifications:

Device Family	Commercial Type No.'s	Slash Sheet
Analog Multipliers	AD534,AD532,4213VM	/139
JFET Analog Switches	DG180 Series, DG190 Series	/111
CMOS Series Analog Switches	5040 Series, DG300 Series, DG200 Series	/105,/116,/123
CMOS Series Analog Multiplexers	DG500 Series,6108,6208,6116,6216	/190
Darlington Transistor Arrays	2001,2002,2003,2004,2005	/141
Regulating Pulse Width Modulators	1524,1525,1526,1527	/126
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ELECTRICAL CHARACTERIZATION

OF

SIGNAL PROCESSING MICROCIRCUITS

SECTION I

INTRODUCTION

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1.1 Objective

The objective of this effort is to conduct characterization efforts for analog integrated circuit device types for inclusion into the MIL-M-38510 specification system (General Specification for Microcircuits). The effort includes determination of a device's parameters and its limits as well as static and dynamic test circuits to verify these limits. All of the characterization and specification efforts performed are guided by the fundamental objectives of MIL-M-38510 specification system which are to achieve quality, reliability, interchangeability, and standardization of microcircuits procured for use in military systems.

1.2 MIL-M-38510 Specification Program

Microcircuit devices for US military systems are procured in accordance with MIL-M-38510, General Specification for Microcircuits and requires device manufacturers to perform specified tests. Furthermore, the device manufacturer must incorporate certain controls and procedures in order to become a qualified source for a particular microcircuit device type. Such device types are specified in individual "slash sheets" and incorporated into the MIL-M-38510 specification system.

1.3 Scope of Report

The scope of the effort includes electrical characterization of the following device types:

a. AD534, AD532, 4213VM analog multipliers
b. 180 J-FET analog switch series
c. 200, 300, 5040 CMOS analog switch series
d. 506-509, 506A-509A CMOS multiplexer series
e. 2000 darlington transistor array series
f. 1524, 1525, 1526, 1527 regulating pulse width modulators
g. TL431 shunt regulating reference

The determination of electrical parameters, limits, and parameter measurement test circuits is the result of government/industry coordination efforts. The JEDEC JC-41 committee on Linear Integrated Circuits formed the coordination basis for the technical categories included in the generated detail specifications. Such cooperative government/industry efforts have resulted in specification

development to satisfy the interests of both parties by specific tailoring of draft detail specification inputs.

MIL-M-38510 slash sheet development based on the results of the government/manufacture interface includes the following:

a. Formulation of Table I, Electrical Performance Characteristics, which specifies the device parameters, test conditions and methods.
b. Formulation of Table II, Electrical Test Requirements; Table III, Group A Inspection; Table IV, Group C Endpoint Electrical parameters.
c. Design of static and dynamic test circuits, functional schematics, terminal connection diagrams, steady-state power and reverse bias burn-in circuits, accelerated burn-in the life test circuits.

1.4 Approach to Charactercation

RADC's approach to characterization has evolved over many years of performing electrical evaluations of analog microcircuits for inclusion into the MIL-M-38510 specification system. Two key factors which influence RADC's decision to begin a characterization effort are listed below in their order of importance:

1. Present or potential usage of device in military systems
2. Level of vendor support

Weighing these factors, RADC will establish a characterization program which upon completion will result in a thorough representation of the device attributes over the full military temperature range. To generate a MIL-M-38510 specification, the characterization plan will perform the following tasks:

a. Obtain a large test sample from all interested vendors, consisting of several different date codes, lots, and variations of the device type series (for example, internal vs. external references on a D/A converter). When acquiring the test sample lots for the evaluation, samples from both vendor and distributors are obtained. Pieces which are procured by RADC are operational over the full military temperature range of -55°C to +125°C, but are not processed to MIL-STD-883 screening requirements. However, test samples obtained from the various

vendors may be screened to MIL-STD-883. Obtaining samples from these two sources allows RADC to view a much broader distribution of parts and thus yielding a more meaningful data base.

b. Develop test hardware/software for the appropriate automatic test system, with one or more test circuit variations. When needed, supplementary bench tests are included for parameters such as very low noise offset voltage or very fast time based measurements.

c. Insure test correlation to independent testers, such as vendor automatic test system, bench top ATE, and bench top test circuits.

d. Develop a complete data base for each test sample lot, which includes all possible static/dynamic parameters over several temperatures, numerous test condition variations, (for example varying power supply voltages, load conditions, source parameters), all possible logic states and power supply turn-on and sequencing. In order to compare test data, vendor data is generally preferred, however, this may not be attainable. Manual bench test data is then obtained, but only as a second choice, since identical test conditions may not be achievable in both the automatic test set-up and the bench test set-up. For example, measurement time on some parameters may cause the device to self-heat, thus significantly affecting the measured data. A measurement accuracy to parameter accuracy ratio of ten to one is desirable. This can be reduced depending on the parameter and the type of measurement. If the desired equipment accuracy is not achievable, the error sources are identified, assessed, and either eliminated or subtracted from the resultant measurement.

e. Perform extensive data reduction and analysis, including graphical comparisons and presentations to highlight the various limit failures. Also, identification of failures by the respective vendor code and lot date code is included. An example of a data reduction technique is the linearity plot shown in Figure 1.

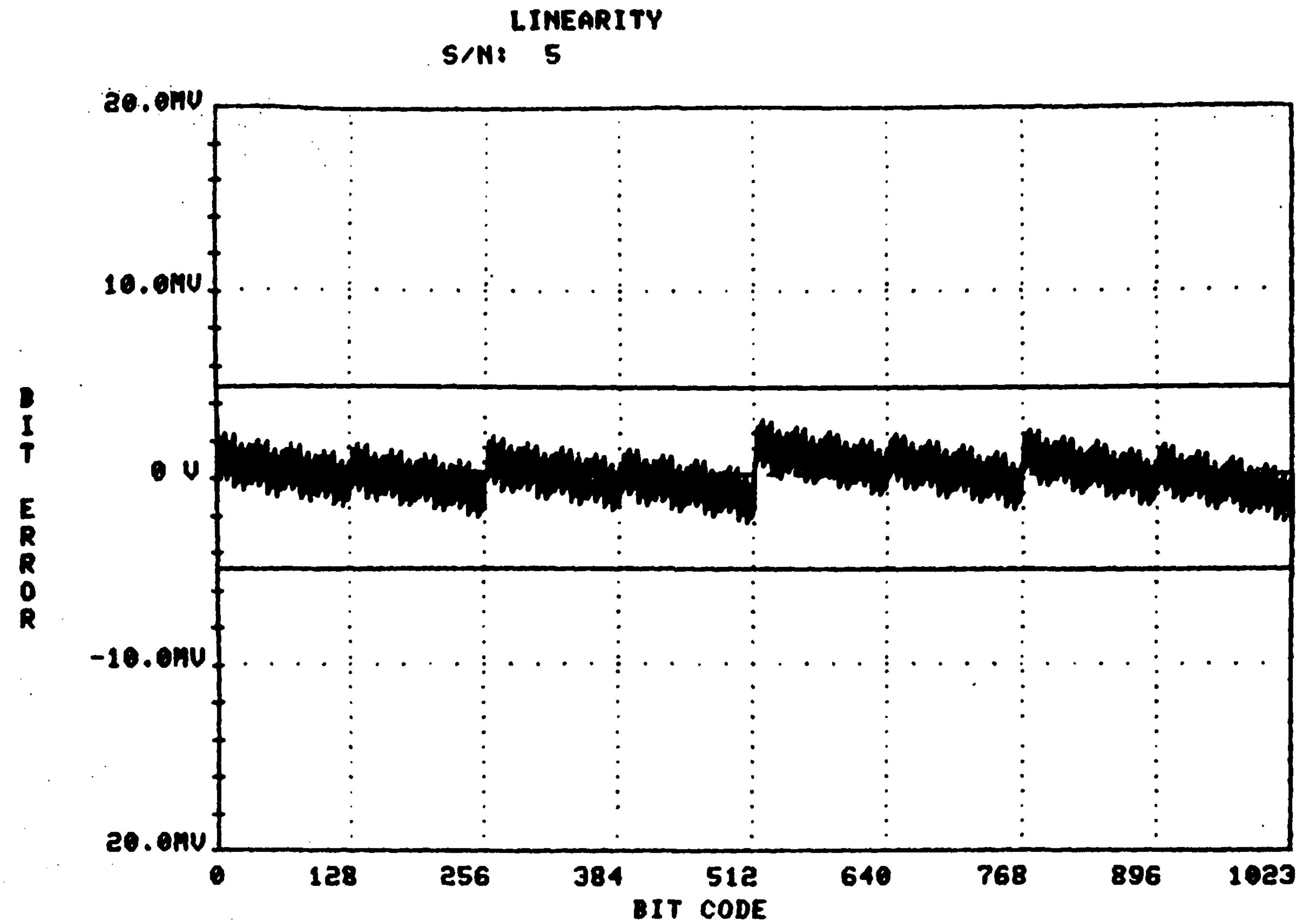
f. Design two or more burn-in and operating life test circuits. These could include burn-in circuits developed and recommended by the devices vendors. Verification and optimization of burn-in circuits are performed through extended

burn-in, life testing, and analysis of all failures. Optimum burn-in circuits selected are then included in the final specification.

g. Generate a MIL-M-38510 specification using the above data to establish the various parametric limits.

h. Negotiate slash sheet test parameters, limits, test methods and circuits, with all device manufacturers and representative users. The characterization data and proposed slash sheet are sent to selected industry and government agencies, as well as reviewed in formal meetings (JC-41) with device vendors. All essential comments are resolved and incorporated into the final draft of the slash sheet that is now ready for full industry/DOD coordination.

When the coordination period ends, RADC will address all questions and comments and the slash sheet will be dated and issued for DOD/industry use.



	WORST CASE POSITIVE ERROR		WORST CASE NEGATIVE ERROR		3-SIGMA POINTS
END POINT	3.164MV AT BIT CODE	519	-2.371MV AT BIT CODE	504	3.513MV
LEAST SQUARES	2.918MV AT BIT CODE	519	-2.619MV AT BIT CODE	504	3.512MV

Figure 1 Linearity Data Reduction Example

SECTION II

INTERNALLY TRIMMED ANALOG MULTIPLIERS

MIL-M-38510/139

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2.1 INTRODUCTION

This section reviews the characterization effort for internally trimmed analog multipliers. Analog multipliers have many applications such as analog signal processing, algebraic/trigonometric function synthesis, and accurate voltage controlled oscillators and filters. The identified need and usage in military systems and manufacturer recommendations were factors in selecting these device types for inclusion in MIL-M-38510 general specifications for microcircuits. Table I lists the internally trimmed analog multipliers specified for MIL-M-38510/139.

TABLE 1 TABLE OF DEVICE TYPES SPECIFIED

Device Type	Generic Type	Manufacturer	Description
13901	AD534T	Analog Devices	1% max. error, 4 quadrant
13902	AD534S	Analog Devices	2% max. error, 4 quadrant
13903	AD532S	Analog Devices	4% max. error, 4 quadrant
13904	4213VM	Burr Browm	4% max. error, 4 quadrant

2.2 DESCRIPTION OF DEVICE TYPES

AD534 Analog Multiplier (Devices 01; 02)

The AD534 is a monolithic laser trimmed four quadrant analog multiplier with an accuracy specification of $\pm$ 1% max (device 01) and $\pm$ 2%max (device 02) for the temperature range of $-55^{\circ}C \leq T_A \leq 125^{\circ}C$. Figure 1 shows the functional block diagram for the AD534. Input voltages are transformed to differential currents by three (3) identical voltage to current converters, with trimmed zero offsets, and inputted into the multiplier cell. The product of the X and Y inputs is performed by the multiplier cell which uses the Gilbert's translinear technique. This product is then scaled to 10V by a 10V "buried zener" which is laser trimmed to provide the overall scale factor (SF). This difference between XY/SF and the Z differential currents are then applied to a high gain output amplifier. The relationship between all inputs is shown in the following equation.

$$V_{out} = A\,(((X1 - X2)\,(Y1 - Y2))/10 - (Z1 - Z2))$$

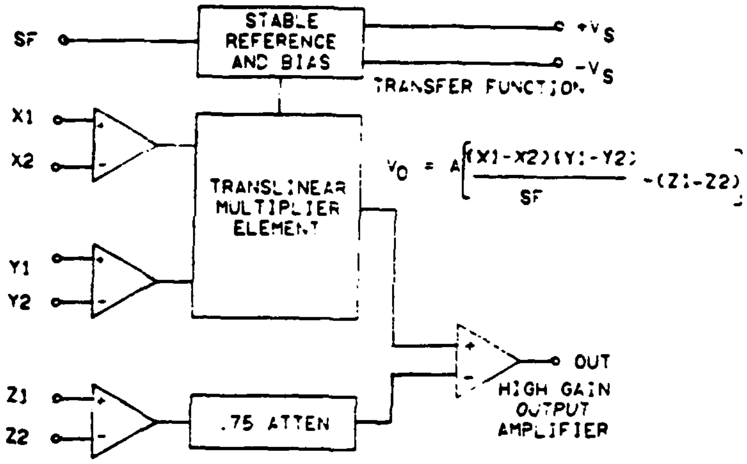


Figure 1 AD534 Functional Block Diagram

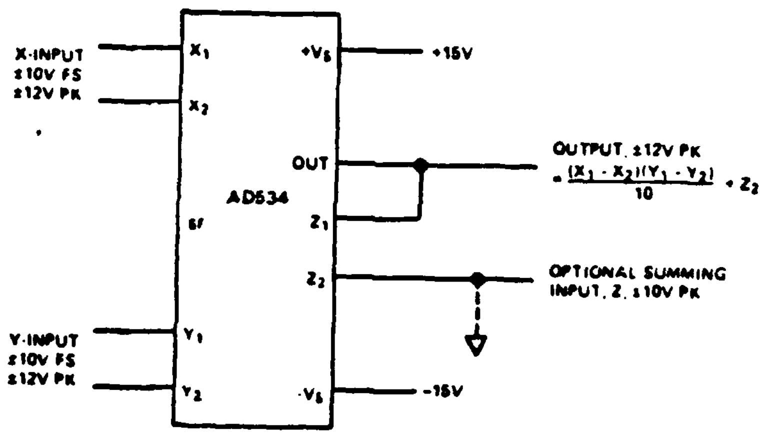


Figure 2 AD534 Analog Multiplier Basic Connection

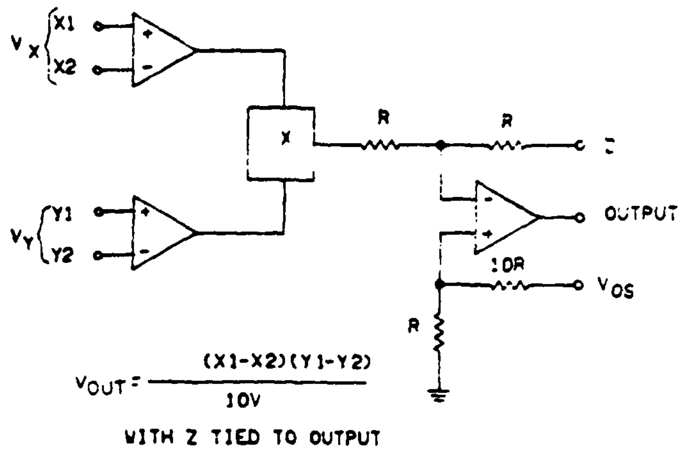


Figure 3 AD532 Functional Block Diagram

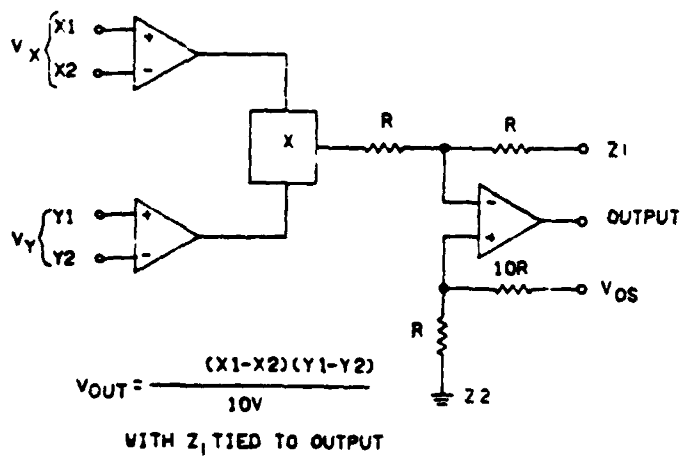


Figure 4 4213 Functional Block Diagram

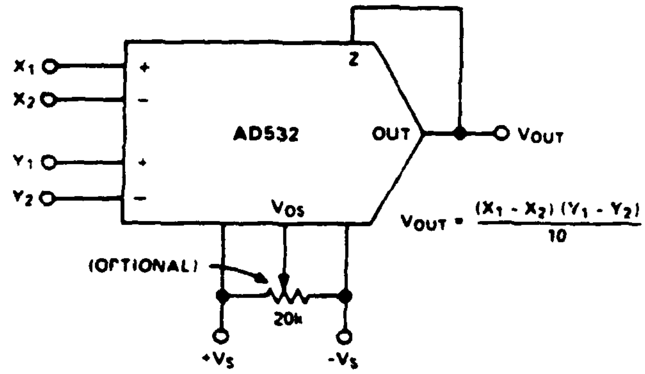


Figure 5 AD532 Analog Multiplier Basic Connection

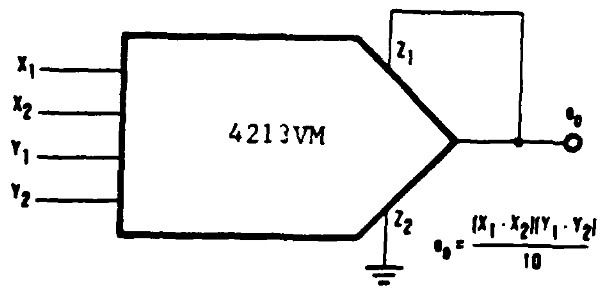


Figure 6 4213 Analog Multiplier Basic Connection

where

A = open loop gain of output amplifier

X, Y, Z = input voltages

Figure 2 shows the basic multiplier connection for the AD534.

AD532, 4213 Analog Multiplier (Devices 03, 04)

The AD532 is a monolithic laser trimmed four quadrant analog multiplier with an accuracy specification of $\pm$ 4% max (device 03) over temperature. The 4213 is a hybrid laser trimmed four quadrant analog multiplier with an accuracy specification of $\pm$4% max (device type 04). For both device types, the X and Y input voltages are fed into high impedance differential amplifiers which transforms the differential input voltages into differential currents. Both X and Y amplifiers offsets are laser trimmed to near zero. The product of the input signals are resolved by the multiplier cell utilizing the Gilbert's linearized transconductance technique. This product then feeds an output amplifier to yield the following output relationship

$$V_{out} = (X1 - X2)(Y1 - Y2)/10$$

Any residual output offset voltages can be zeroed by utilizing the V_{OS} terminal and applying the necessary dc voltage. Figures 3 and 4 show the functional schematics for device 03 and 04 respectively. Figures 5 and 6 shows the basic multiplier connections for device 03 and 04.

2.3 TEST DEVELOPMENT

A listing of the multiplier parameters tested to characterize device types 01 thru 04 are given in Table 2. Table 3 shown in the appendix lists the min/max limits and some of the test conditions used for these parameters.

TABLE 2 TEST PARAMETERS FOR CHARACTERIZATION

Item	Symbol	Parameter
1	MA_{XY}	Multiplier Accuracy
2	$MA_{XY/T}$	Multiplier Accuracy Drift

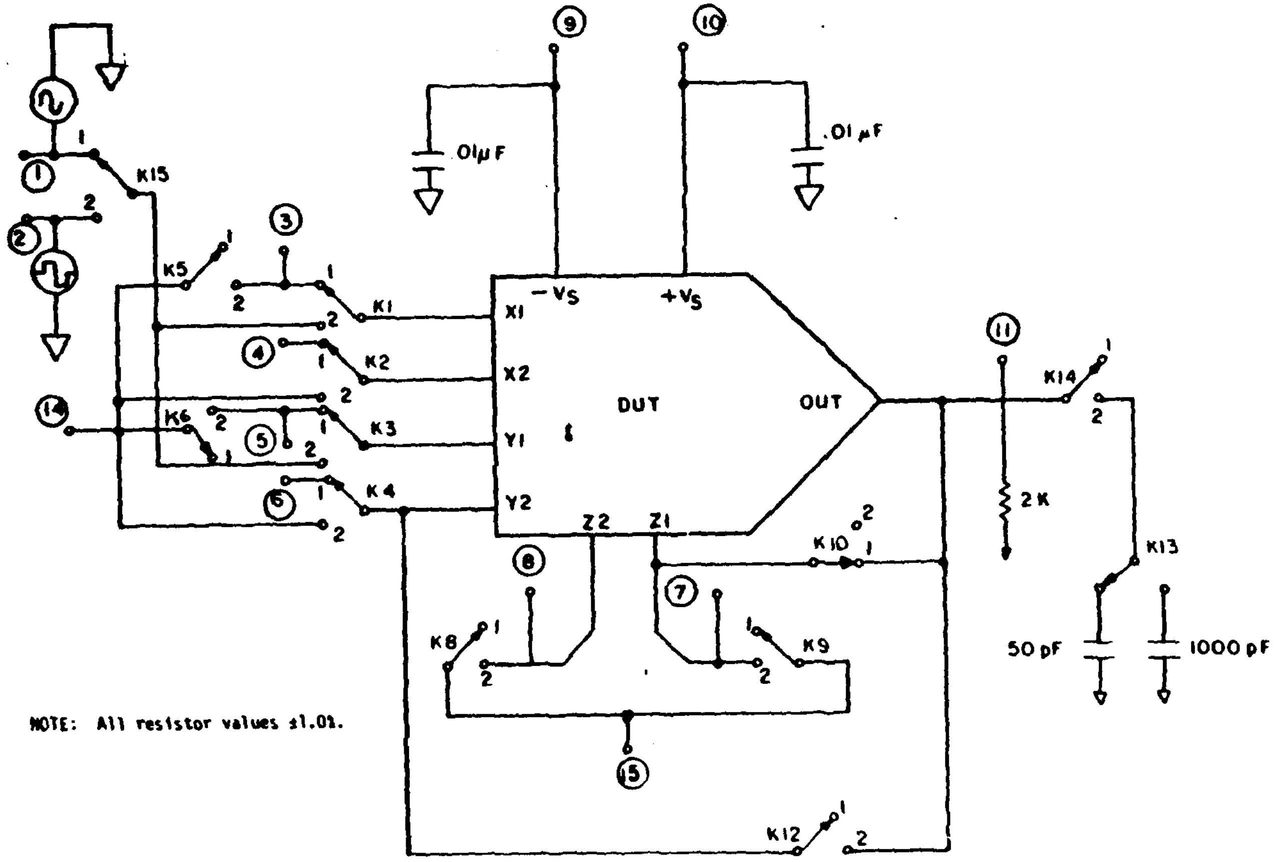
3	V_{OIO}	Output Offset Voltage
4	$V_{OIO}/\ T$	Output Offset Voltage Drift
5	$V_{IO(x)}$, $V_{IO(y)}$, ($V_{IO(z)}$)	Input Offset Voltage ($V_{IO(z)}$device 01, 02 only)
6	$V_{IO}/\ \ T$	Input Offset Voltage Drift
7	$+I_{IB}$, $-I_{IB}$, ($I_{IB(Z)}$)	Input Bias Current (I_{IB}(Z) device 03 only)
8	$I_{OS(+)}$, $I_{OS(-)}$	Output Short Circuit Current
9	I_{cc}, I_{ee}	Supply Currents
10	CMRR(X), CMRR(Y), (CMRR(Z))	Common Mode Rejection (CMRR(Z) devices 01,02,only)
11	V_{OP}	Output Voltage Swing
12	PSRR1, PSRR2	Power Supply Rejection Ratio
13	ts(+), ts(-)	Settling Time
14	SR(+), SR(-)	Slew Rate
15	FT_X, FT_Y	Feedthrough
16	AE_X, AE_Y	Small Signal Amplitude Error
17	NL_X, NL_Y	Nonlinearity
18	$NI_{(BB)}$	Wideband Noise

Test Philosophy:

The approach to testing was to study typical parameters on a bench top test set-up in conjunction with automatic testing on the Tektronix S3270. The objective of this dual approach was to achieve confidence in testing and to identify anomalies inherent to the analog multipliers.

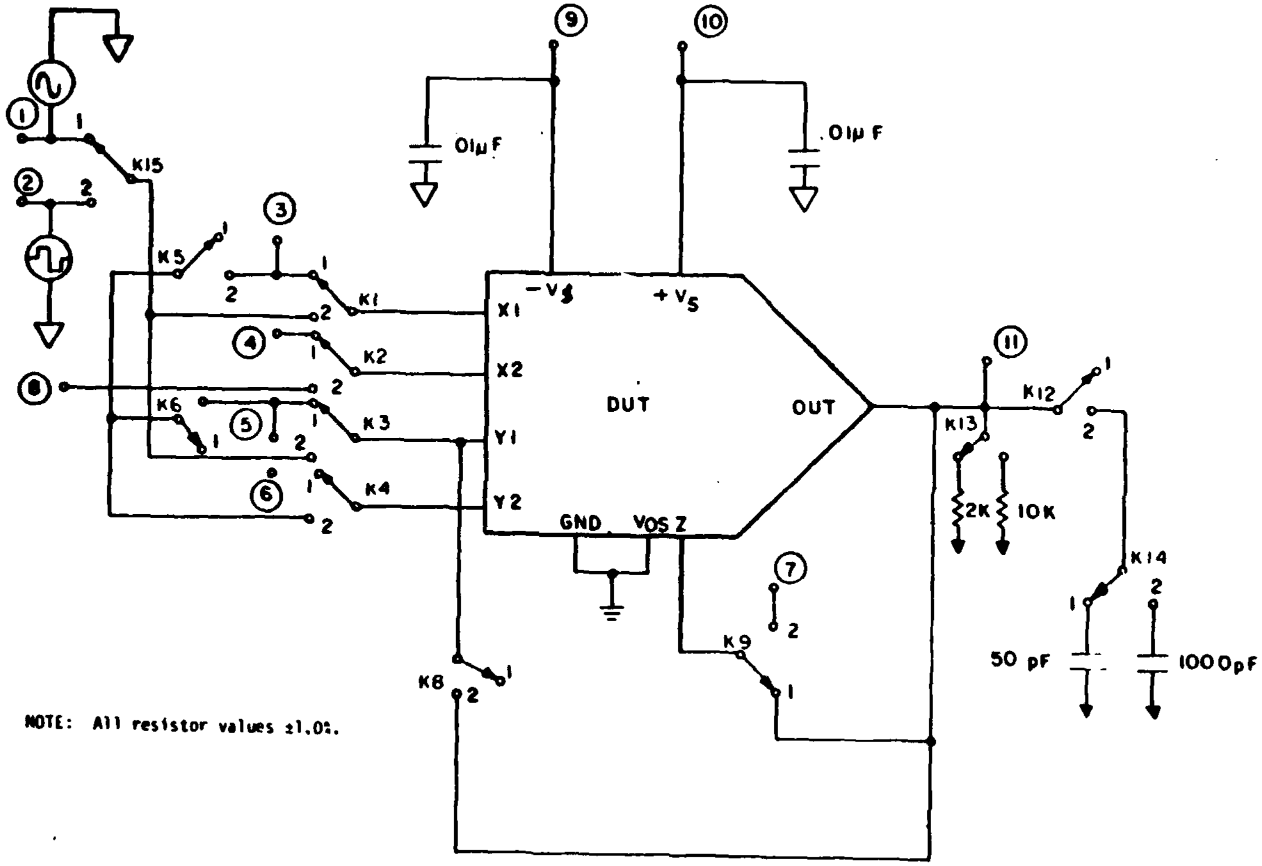
Test Circuits:

The static and dynamic test circuit schematics used to measure the analog multiplier parameters are shown in Figures 7 and 8. All relays are shown in the normally de-energized position. All the parameters can be measured automatically except for settling time, small signal amplitude error, and wideband noise. The settling time test and small signal amplitude error test were performed on the bench. The settling time test requires an oscilloscope to determine how fast the analog multiplier settles to within 2% of it's final value. The small signal amplitude error test requires an oscilloscope to determine when the amplitude of 2Vpp sinewave is reduced by 1%. The wideband noise test was also done on the bench because of the design considerations necessary, and the need of a filter to establish the bandwidth. Schematic diagrams for the wideband noise test circuits are shown in Figures 9 and 10.



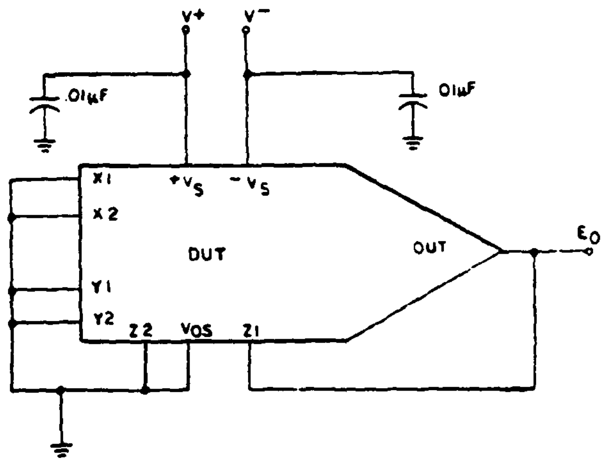
NOTE: All resistor values ±1.0%.

Figure 7 AD534 Static and Dynamic Test Circuit



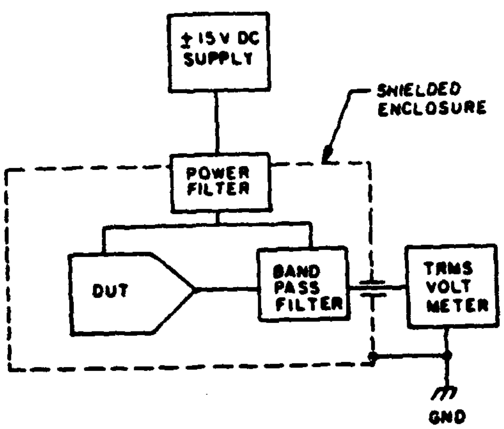
NOTE: All resistor values ±1.0%.

Figure 8 AD532/4213 Static and Dynamic Test Circuit



NOTE. E_O is measured using a rms voltmeter with a bandwidth of 10 Hz to 100 kHz.

Figure 9 Wideband Noise Test Circuit



NOTES:
1. Bandpass filter:
   Passband gain = 40 dB ±0.5 dB.
   Fc low = 10 Hz ±1 Hz.
   Fc high = 100 kHz ±10 kHz.
   Attenuation slope = 12 dB/Oct.
2. V_{NOISE} = Reading/100
3. Voltmeter: HP3400A or equivalent.
4. ±15 V dc power supply HP6235A or equivalent.

Figure 10 Noise Measurement Block Diagram

2.4 TEST RESULTS AND DATA

A total of 88 devices were tested covering all three device types. Forty 532S parts, thirty-three 534S, ten 534T, and five 4213 parts were tested for all static and dynamic parameters.

Parts identification is as follows:

Type	S/N	Package
532S	1176-1195	TO-100, 10-pin can
532S	34 - 53	TO-116, 14-pin DIP
534S	54 - 73	TO-100, 10-pin can
534S	1-9, 4537, 4538, 4595, 4596, 4600	TO-116, 14-pin DIP
534T	1 - 10	TO-100, 10-pin can
4213	1 - 5	TO-100, 10 pin can

Data sheets generated on the Tektronix S3270 are shown in the appendix. All of the data is within limits unless an asterik and the letter A or B are displayed adjacent to the measured value. Asterik A meaning that the limit is above specification and asterik B meaning that the limit is below specification. The data is shown with three temperatures of -55°C, 25°C, and 125°C adjacent to each other. This allows the user to readily determine temperature variations in data. It should be noted that X and Y nonlinearity data is displayed separately. This was done because X and Y nonlinearity was originally done dynamically. Data is shown with all the parameters needed to perform the necessary calculations for X and Y nonlinearity. These equations will be discussed in a later section of the technical report (Test Calculations).

2.5 DISCUSSION OF RESULTS

For each parameter tested, the yields were generally very good with surprisingly few errors. At +25°C for both the 532's and 534's, the errors were due to the tighter limits at +25°C. For the 4213's, most errors were observed at 25°C and 125°C.

Multiplier Accuracy (MA_{XY})

Most multiplier accuracy errors for both 534 and 532 occured in the second and fourth quadrants ($MA_{X^-Y^+}$, $MA_{X^+Y^-}$). The only errors observed in the first and third quadrants were by generic type 532. Generic device type 4213 passed all multiplier accuracy tests. The yields for all device types was greater than 95%. It should be noted that the error increases over temperature for first and fourth quadrant multiplication and decreases for second and third quadrant multiplication.

Multiplier Accuracy Drift ($MA_{XY}/\Delta T$)

All device types produced a 100% yield for both -55°C and +125°C. Data taken on the 534 T devices (device 01) was 25% better than the limit. Data on the 534S and 532S devices were 50% better than the specified limit. Data on the 4213V devices was 50% better than the specified limit.

Output Offset Voltage (V_{OIO})

This parameter was passed by all device types, according to their specified limits. All measurements of this parameter for 534T devices were 50% better than specified, for 534S devices 60% better, and for 532S and 4213V devices, the data measured was exactly as specified.

Output Offset Voltage Drift ($V_{OIO}/\Delta T$)

All device types tested produced a 100% yield. Upon examination of data, no temperature trends were observed for any of the three device types tested. Output offset voltage increased with temperature for one device and decreased with temperature for another device in the same lot. Drift measurements for the 534T, 534S, 532S, and 4213V devices were as specified.

Offset Voltage ($V_{IO}(X)$, $V_{IO}(Y)$, $V_{IO}(Z)$)

The offset voltage measurement is a calculation of three different measurements which takes into effect the feedthrough errors and output offset error. Device types 01 and 02 both had yields of better than 95% with device type 03 (532S) having slightly less than 95% yield. Device type 04 (4213V) had a yield of 100%.

Offset Voltage Drift ($V_{IO}(X)/\Delta T$, $V_{IO}(Y)/\Delta T$, $V_{IO}(Z)/\Delta T$)

All 88 devices tested for generic types 534T, 534S, 532S, and 4213V passed this parameter to achieve 100% yield. As in the output offset voltage measurement, no temperature trends were observed.

Input Bias Current (I_{IB})

Measurements taken on this parameter showed a 100% yield for the four generic types. The measurements for $+I_{IB}$, $-I_{IB}$, and $I_{B(Z)}$ (for 532 only), were 50% better than the vendor agreed upon limit. As can be seen in the appendix, input bias currents increase as the temperature is reduced.

Input Offset Current (I_{IO})

Input offset current was obtained by subtracting the minus input bias current ($-I_{IB}$) from the plus input bias current ($+I_{IB}$). Yields on this parameter were very good with generic type 532S achieving a yield of 90%, 534S a 97% yield, 534T a yield of 80%, and 4213V a yield of 100%. The low yield for the 534T devices was due to the small lot size of 10. All errors except for one occured at $-55^{o}C$.

Output Short Circuit Current (I_{OS})

Output short circuit current was measured with the output shorted to ground for a time less than 25 milli-seconds. The yield was 100% for all four device types over temperature. In all cases, data measured was on the average of 10mA less than the specified limit. Output short circuit current increases as temperature decreases.

Supply Current (I_{cc}, I_{ee})

The vendor recommended limit for this parameter was 6.0 mA maximum. After characterization, it was agreed to raise the maximum to 6.5 mA for all four device types. All 88 parts that were tested passed this limit. It should be noted that supply current increases slightly as temperature increases.

Common Mode Rejection Ratio (CMRR)

This parameter was passed by all four device types over the three temperature ranges. Characterization data showed that on the average common-mode rejection was 20db higher than the minimum specified limit.

Output Voltage Swing (V_{OP})

All 83 devices tested, covering generic types 534T, 534S, and 532S passed this parameter to the specified limit. The data obtained, showed that generic type 534 output voltage swing in the minus direction differed from generic type 532 over temperature. For the 534's the output voltage minus parameter decreased as temperature increased, conversely the 532's minus output voltage swing increased as temperature increased. The positive output voltage swing parameter increased as temperature increased for both the 534's and 532's. When characterizing this parameter for generic device type 4213, all devices failed. Upon discussions with Burr Brown, RADC was informed that +15V on input would overdrive the multiplier and caused an inversion at the output. RADC reduced the input conditions to +11V and all parts passed.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio parameter was specified by the vendor for generic type 532 but not for generic type 534. RADC proposed limits of 100mV/V for supply voltages ranging from ± 12V to ± 15V (PSRR1) and 4.0mV/V for supply voltages of ± 15V to ± 18V (PSRR2) for generic type 534. Proposed limits for generic type 532 were 280 mV/V for supply voltages ranging from ± 12V to ± 15V and ± 40 mV/V for ranges from ± 15V to ± 18V. Upon discussion with the vendor, the supply voltage range for the PSSR1 parameter was changed to ± 13.5V to ± 15V. Device type 04 exhibited the same behavior as the 03 device. The limit was set to 10mV/V for device types 01 and 02 and 50 mV/V for device type 03 and 04. All four device types passed these limits over temperature.

Settling Time (ts(+), ts (-))

Settling time was measured by the circuit in Figure 11 at 25°C. All parts tested for the four device types, passed this parameter according to their specified limits. Examination of the data showed that for generic type 534, ts(+) was on the average 500ns slower than ts(-). No such trends were observed for generic type 532 and generic type 4213.

Slew Rate (SR(-), SR(+))

Slew rate was measured by same circuit as settling time (Figure 11) but was done at -55°C and +125°C as well as at 25°C. Device types 01 and 02 had a yield of 100%. On the average slew rates were 5 volts per microsecond faster than the specified limit. Device type 03 had a yield of 90%. Device failures occurred at 55°C and were only marginal (5 volts per microsecond slower). Device type 04 had a 100% yield. For all four device types slew rate increased as the temperature increased.

Feedthrough (FT_X, FT_Y)

The yield for this parameter was 100% for all four device types. From the data obtained, all the parts tested had values at least 50% better than the specified limit. The higher limits remained due to the vendor's concern that tighter limits would severely reduce yields. No temperature trends were observed.

Small Signal Amplitude Error (AE_X, AE_Y)

Small signal amplitude error was measured at 25°C and had a yield of 95% or better for all four device types. On the average, data obtained showed that measurements were 20kHz above the specified limits which is 75kHz for device types 01 and 02 and 70kHz for device types 03 and 04. All failures were marginal and observed when the SSAE(Y) parameter was measured.

Nonlinearity (NL_X, NL_Y)

This test was originally done at 25°C and measured by an A.C. test circuit utilizing a sine wave generator and an oscilloscope configured in the X-Y mode. On vendor request, and verification by RADC, this test was changed to a D.C. test and measured over temperature. Generic type 534 was measured utilizing the 3-point method, generic type 532 and generic type 4213V utilize the 5-point method. Correlation and calculations between the two methods will be discussed later in the technical report. Yields were generally good for all four device types.

Wideband Noise ($N_{I(BB)}$)

This parameter was measured at 25°C with a bandwidth from 10Hz to 100kHz. All devices covering the four device types passed this parameter as specified. Generally, measured values were 5uVrms smaller than the specified limit.

2.6 TEST CALCULATIONS

Feedthrough:

The equations to calculate the feedthrough error for both the X and Y amplifier are as follows:

$$FTx = ((XFP + XFM)/2) - V_{OIO}$$

and

$$FTy = ((YFP + YFM)/2) - V_{OIO}$$

where:

XFP = Feedthrough error for plus terminal of the X amplifier
(Input conditions: X = 10, Y = 0)

XFM = Feedthrough error for minus terminal of the X amplifier
(Input conditions: X = -10, Y = 0)

XFP = Feedthrough error for plus terminal of the Y amplifier
(Input conditions: X = 0, Y = 10)

XFM = Feedthrough error for minus terminal of the Y amplifier
(Input conditions: X = 0, Y = -10)

V_{OIO} = Output offset error
(Input conditions: X = 0, Y = 0)

Feedthrough error is defined as the output voltage of the multiplier when either input is at zero volts. Theoretically, when either input is at zero, the output should be zero, but a certain fraction of the non-zero input will "feed through" and appear at the output. It should be noted that feedthrough error will increase as the frequency on the nonzero input signal increases. This test was originally a dynamic test but was changed to a static test. This was done per the vendor's request and upon verification and validity of the equations by RADC. As can be seen in the equations both extremes are measured and averaged with one input at zero to achieve feedthrough worst case errors. The output offset voltage is subtracted to nullify any errors due to the output summing amp which is internal to the analog multiplier.

Nonlinearity:

The equations to calculate the X and Y nonlinearity parameter are different between generic type 534 and generic types 532 and 4213. This is because of the nonlinearity wave shape between the two types being different. Generic type 534 has a parabolic nonlinearity wave shape and generic type 532 and 4213 have a sinusoidal wave shape. Like feedthrough this test was originally done dynamically, but was changed to a static test. The equations for X and Y nonlinearity for generic type 534 are as follows:

$+NL_x = (((ERR1 + ERR4)/2) - YFP)/2$

$-NL_x = (((ERR2 + ERR3)/2) - YFM)/2$

$+NL_y = (((ERR1 + ERR2)/2) - XFP)/2$

$-NL_y = (((ERR3 + ERR4)/2) - XFM)/2$

where:

ERR1 = Multiplier accuracy (X = +10, Y = +10)

ERR2 = Multiplier accuracy (X = +10, Y = -10)

ERR3 = Multiplier accuracy (X = -10, Y = +10)

ERR4 = Multiplier accuracy (X = -10, Y = -10)

YFP, YFM, XFP, XFM = defined in feedthrough calculation.

This is known as the three-point test method.

The equations for X and Y nonlinearity for generic types 532 and 4213 are the same as the 534 plus the following.

$+NL_x(A) = ERR10-(ERR4-ERR1)/4+(((ERR4+ERR1)/2)+YFP)/2$

$+NL_x(B) = ERR12+(ERR4-ERR1)/4+(((ERR4+ERR1)/2)+YFP)/2$

$-NL_x(A) = ERR9-(ERR3-ERR2)/4+(((ERR3-ERR2)/2)+YFM)/2$

$-NL_x(B) = ERR11+(ERR3-ERR2)/4+(((ERR3+ERR2)/2)+YFM)/2$

$+NL_y(A) = ERR6-(ERR2-ERR1)/4+(((ERR2+ERR1)/2)+XFP)/2$

$+NL_y(B) = ERR8+(ERR2-ERR1)/4+(((ERR2+ERR1)/2)+XFP)/2$

$-NL_y(A) = ERR7-(ERR4-ERR1)/4+(((ERR4+ERR1)/2)+XFM)/2$

$-NL_y(B) = ERR5-(ERR4-ERR1)/4+(((ERR4+ERR1)/2)+XFM)/2$

where:

ERR5 = Multiplier accuracy (X = -10, Y = -5)

ERR6 = Multiplier accuracy (X = +10, Y = -5)

ERR7 = Multiplier accuracy (X = -10, Y = +5)

ERR8 = Multiplier accuracy (X = +10, Y = +5)

ERR9 = Multiplier accuracy (X = -5, Y = -10)

ERR10 = Multiplier accuracy (X = -5, Y = +10)

ERR11 = Multiplier accuracy (X = +5, Y = -10)

ERR12 = Multiplier accuracy (X = +5, Y = +10)

All other terms are defined in previous calculations.

These equations will be explained by the use of Figure 12 and the equation that applies to it.

To determine the $+NL_X(A)$ error, Figure 12 is used with this equation

$$+NL_X(A) = \underbrace{ERR10-(ERR4-ERR1)/4}_{J}+\underbrace{(((ERR4+ERR1)/2)+YFP)/2}_{K}$$

As can be seen, this equation is divided into three basic sections. The J section is the slope of the line drawn from the endpoints measured. The K section is the factor used to center the curve around the X axis. The variable ERR10 is the location (X = -5, Y = +10) in which the nonlinearity error of interest is measured. All the other equations are based on the same principles as discussed here.

2.7 CONCLUSIONS AND RECOMMENDATIONS

Generic types 534, 532, and 4213 are accurate analog multipliers when multiplying signals between -10V and +10V. This accuracy can be improved by designing with potentiometers to trim for accuracies needed at specific voltage ranges. If potentiometers are used, it should be noted that accuracies at different ranges will be affected.

Both vendors advertise that the 534, 532, and 4213 can be configured to do divider functions and square-root functions. It is recommended that these devices not be used in those configurations. During characterization, it was found that the accuracy of the divider and square-root functions greatly diminishes over temperature.

The testing of nonlinearity was changed from a dynamic test to a static test to reduce the cost of testing. The static test in itself will not give the worst case nonlinearity error but it does guarantee that the error is within 10% of the value measured. If the user is interested in the exact worst case error and the curve it follows, it is recommended that they use the dynamic test circuit shown in Figure 12.

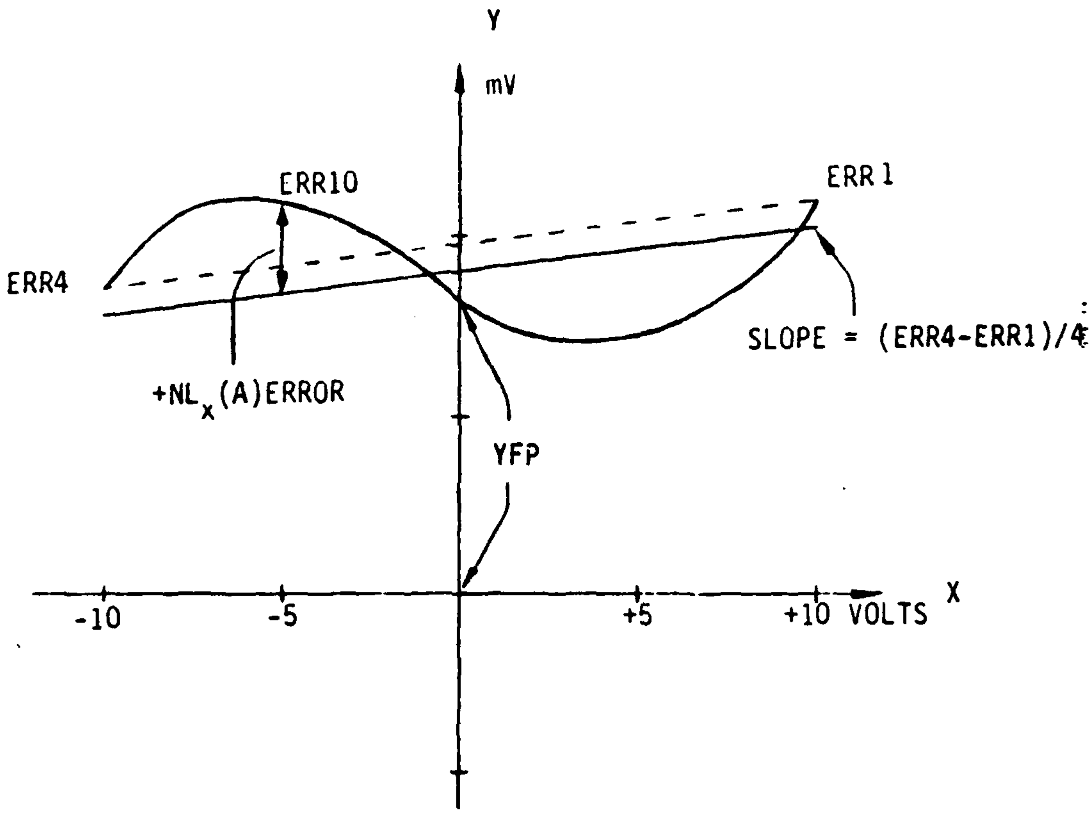
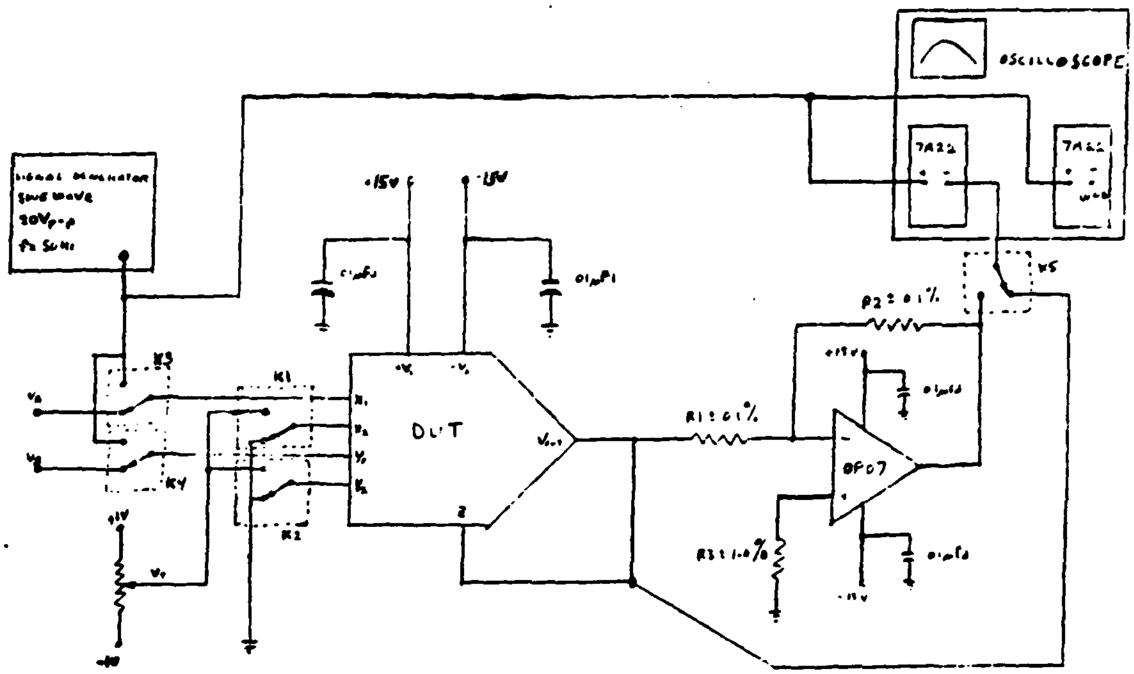


Figure 11 Nonlinearity Error Waveform



TEST	ADAPTER PINS VA	VB	VT	ENERGIZED RELAYS	VALUE	UNIT
+NLx	20Vpp	+10V	TRIM	K2,K3	Vmax	mV
-NLx	20Vpp	-10V	TRIM	K2,K3,K5	Vmax	mV
+NLy	+10v	20Vpp	TRIM	K1,K4	Vmax	mV
-NLy	-10V	20vpp	TRIM	K1,K4,K5	Vmax	mV

Figure 12 Nonlinearity Error Bench Test Circuit

2.8 BIBLIOGRAPHY

a. Nonlinear Circuits Handbook, Analog Devices (1976)

b. Analog Devices Integrated Circuits Data Book (1984)

c. Electronic Circuits: Digital and Analog, Charles A. Holt, (1978)

2.9 APPENDIX

Table 2-3 lists the test parameters for device types 01-04 as well as test conditions and min/max limits.

532 and 534 analog multiplier data sheets generated on the Tektronix 3270 are shown in Table 2-4.

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Device 01 Min	Limits Device 01 Max	Limits Device 02 Min	Limits Device 02 Max	
Multiplier accuracy (-x)(-y)	MAx-y-	Vx = -10 V	$T_A = 25°C$	-0.5	0.5	-1.0	1.0	%FS
		Vy = -10 V	$-55°C \leq T_A \leq 125°C$	-1.0	1.0	-2.0	2.0	
Multiplier accuracy (-x)(+y)	MAx-y+	Vx = -10 V	$T_A = 25°C$	-0.5	0.5	-1.0	1.0	"
		Vy = +10 V	$-55°C \leq T_A \leq 125°C$	-1.0	1.0	-2.0	2.0	
Multiplier accuracy (+x)(-y)	MAx+y-	Vx = +10 V	$T_A = 25°C$	-0.5	0.5	-1.0	1.0	"
		Vy = -10 V	$-55°C \leq T_A \leq 125°C$	-1.0	1.0	-2.0	2.0	
Multiplier accuracy (+x)(+y)	MAx+y+	Vx = +10 V	$T_A = 25°C$	-0.5	0.5	-1.0	1.0	"
		Vy = +10 V	$-55°C \leq T_A \leq 125°C$	-1.0	1.0	-2.0	2.0	
Multiplier accuracy drift	$MA\frac{xy}{\Delta T}$	Vx = ±10 V Vy = ±10 V	$-55°C \leq T_A \leq 125°C$	-0.01	0.01	-0.02	0.02	$\frac{\%FS}{°C}$
Output offset voltage	V_{OIO}	Vx = Vy = Vz = 0	$T_A = 25°C$	-15.0	15.0	-30.0	30.0	mV
			$T_A = -55°C$	-39.0	39.0	-70.0	70.0	
			$T_A = 125°C$	-45.0	45.0	-80.0	80.0	
Output offset voltage drift	$\frac{V_{OIO}}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-300.0	300.0	-500.0	500.0	$\frac{\mu V}{°C}$
Offset voltage (x)	$V_{IO}(x)$		$T_A = 25°C$	-10.0	10.0	-20.0	20.0	mV
			$T_A = -55°C$	-22.0	22.0	-36.0	36.0	
			$T_A = 125°C$	-25.0	25.0	-40.0	40.0	
Output offset voltage drift (x)	$\frac{V_{OIO}(x)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-150.0	150.0	-200.0	200.0	$\frac{\mu V}{°C}$
Offset voltage (y)	$V_{IO}(y)$		$T_A = 25°C$	-10.0	10.0	-20.0	20.0	mV
			$T_A = -55°C$	-22.0	22.0	-36.0	36.0	
			$T_A = 125°C$	-25.0	25.0	-40.0	40.0	

Table 3. Electrical Parameter Limits Device Type 01 and 02

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Device 01 Min	Device 01 Max	Device 02 Min	Device 02 Max	
Offset voltage drift (y)	$\frac{V_{IO}(y)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-150.0	150.0	-200.0	200.0	$\frac{\mu V}{°C}$
Offset voltage (z)	$V_{IO}(z)$		T_A = 25°C	-15.0	15.0	-30.0	30.0	mV
			T_A = -55°C	-39.0	39.0	-70.0	70.0	
			T_A = 125°C	-45.0	45.0	-80.0	80.0	
Offset voltage drift (z)	$\frac{V_{IO}(z)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-300.0	300.0	-500.0	500.0	$\frac{\mu V}{°C}$
Input bias current (+)	$+I_{IB}$		T_A = -55°C	-2.5	2.5	-2.5	2.5	µA
			25°C $\leq T_A \leq$ 125°C	-2.0	2.0	-2.0	2.0	
Input bias current (-)	$-I_{IB}$		T_A = -55°C	-2.5	2.5	-2.5	2.5	"
			25°C $\leq T_A \leq$ 125°C	-2.0	2.0	-2.0	2.0	
Input offset current	I_{IO}		T_A = -55°C	-300.0	300.0	-300.0	300.0	nA
			25°C $\leq T_A \leq$ 125°C	-250.0	250.0	-250.0	250.0	
Output short circuit current (+)	$I_{OS}(+)$	R_L = 0; t $\leq$25 ns	-55°C $\leq T_A \leq$ 25°C	-40.0		-40.0		mA
			T_A = 125°C	-30.0		-30.0		
Output short circuit current (-)	$I_{OS}(-)$	R_L = 0; t $\leq$25 ns	-55°C $\leq T_A \leq$ 25°C		50.0		50.0	"
			T_A = 125°C		38.0		38.0	
Supply current (+)	I_{CC}	R_L = 00	-55°C $\leq T_A \leq$ 125°C		6.5		6.5	"
Supply current (-)	I_{EE}	R_L = 00	-55°C $\leq T_A \leq$ 125°C	-6.5		-6.5		"
Common mode rejection ratio (x)	CMRR(x)	-10 V $\leq$Vx $\leq$+10 V Vy = +10 V	T_A = -55°C	65.0		54.0		dB
			25°C $\leq T_A \leq$ 125°C	70.0		60.0		
Common mode rejection ratio (y)	CMRR(y)	-10 V $\leq$Vy $\leq$+10 V Vx = +10 V	T_A = -55°C	65.0		54.0		"
			25°C $\leq T_A \leq$ 125°C	70.0		60.0		"

Table 3. (cont.)

Characteristics	Symbol	Conditions $V_S = \pm15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Device 01 Min	Max	Device 02 Min	Max	
Common mode rejection ratio (z)	CMRR(z)	-10 V $\le V_y \le +10$ V	$T_A = -55°C$	65.0		54.0		dB
		$V_x = +10$ V	$25°C \le T_A \le 125°C$	70.0		60.0		
Output voltage swing	V_{OP}		$-55°C \le T_A \le 125°C$	+11.0		+11.0		V
					-11.0		-11.0	
Power supply rejection ratio (-)	PSRR1	14.0 V $\le V_S \le +15$ V, $V_y = +10$ V, $V_x = 10$ V	$-55°C \le T_A \le 125°C$	-1.0	1.0	-1.0	1.0	mV/V
Power supply rejection ratio (+)	PSRR2	±15 V $\le V_S \le \pm18$ V, $V_x = 10$ V, $V_y = +10$ V	$-55°C \le T_A \le 125°C$	-4.0	4.0	-4.0	4.0	"
Settling time (+)	ts(+)	See figure 5	$T_A = 25°C$		3.0		3.0	µs
Settling time (-)	ts(-)	See figure 5	$T_A = 25°C$		3.0		3.0	"
Slew rate (+)	SR(+)		$-55°C \le T_A \le 125°C$	18.0		18.0		V/µs
Slew rate (-)	SR(-)		$-55°C \le T_A \le 125°C$	"		"		"
Feedthrough (x)	FTx		$-55°C \le T_A \le 125°C$	-35.0	35.0	-60.0	60.0	mV
Feedthrough (y)	FTy		$-55°C \le T_A \le 125°C$	-12.0	12.0	-24.0	24.0	"
Small signal amplitude error (x)	AEx	$V_x = 2$ V (p-p) $C_C = 1000$ pF, $V_y = +10$ V 1% error	T_A 25°C	75.0		75.0		kHz
Small signal amplitude error (y)	AEy	$V_y = 2$ V(p-p) $C_C = 1000$ pF, $V_x = +10$ V 1% error	T_A 25°C	"		"		"
Nonlinearity (x)	NLx		$-55°C \le T_A \le 125°C$	-0.3	0.3	-0.5	0.5	%FS
Nonlinearity (y)	NLy		$-55°C \le T_A \le 125°C$	-0.15	0.15	-0.2	0.2	"
Wideband noise	NI(BB)		$T_A = 25°C$		1.5		1.5	mV rms

Table 3. (cont.)

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Min	Max	Unit
Multiplier accuracy (-x)(-y)	MAx-y-	Vx = -10 V	$T_A = 25°C$	-1.0	1.0	%FS
		Vy = -10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy (-x)(+y)	MAx-y+	Vx = -10 V	$T_A = 25°C$	-1.0	1.0	"
		Vy = +10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy (+x)(-y)	MAx+y-	Vx = +10 V	$T_A = 25°C$	-1.0	1.0	"
		Vy = -10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy (+x) (+y)	MAx+y+	Vx = +10 V	$T_A = 25°C$	-1.0	1.0	"
		Vy = +10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy drift	$MA \frac{xy}{\Delta T}$	Vx = ±10 V Vy = ±10 V	$-55°C \leq T_A \leq 125°C$	-0.04	0.04	$\frac{\%FS}{°C}$
Output offset voltage	V_{OIO}	Vx = Vy = Vz = 0	$T_A = 25°C$	-30.0	30.0	mV
			$T_A = -55°C$	-190.0	190.0	
			$T_A = 125°C$	-230.0	230.0	
Output offset voltage drift	$\frac{V_{OIO}}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-2.0	2.0	$\frac{mV}{°C}$
Offset voltage (x)	$V_{IO}(x)$		$T_A = 25°C$	-50.0	50.0	mV
			$T_A = -55°C$	-100.0	100.0	
			$T_A = 125°C$	-100.0	100.0	
Output offset voltage drift (x)	$\frac{V_{OIO}(x)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-800 0	800.0	$\frac{\mu V}{°C}$
Offset voltage (y)	$V_{IO}(y)$		$T_A = 25°C$	-50.0	50.0	mV
			$T_A = -55°C$	-100.0	100.0	
			$T_A = 125°C$	-100.0	100.0	

Table 3. Electrical Parameter Limits Device Type 03

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Min	Max	Unit
Offset voltage drift (y)	$\frac{V_{IO}(y)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-800.0	800.0	$\frac{\mu V}{°C}$
Input bias current (z)	$I_{IB}(z)$		-55°C $\leq T_A \leq$125°C	-12.0	12.0	µA
Input bias current (+)	$+I_{IB}$		T_A = -55°C	-4.0	4.0	"
			25°C $\leq T_A \leq$125°C	-2.0	2.0	
Input bias current (-)	$-I_{IB}$		T_A = -55°C	-4.0	4.0	"
			25°C $\leq T_A \leq$125°C	-2.0	2.0	
Input offset current	I_{IO}		T_A = -55°C	-400.0	400.0	nA
			25°C $\leq T_A \leq$125°C	-200.0	200.0	
Output short circuit current (+)	$I_{OS}(+)$	R_L = 0	-55°C $\leq T_A \leq$25°C	-45.0		mA
			T_A = 125°C	-30.0		
Output short circuit current (-)	$I_{OS}(-)$	R_L = 0	-55°C $\leq T_A \leq$25°C		30.0	"
			T_A = 125°C		"	
Supply current (+)	I_{CC}	$R_L = \infty$	-55°C $\leq T_A \leq$125°C		6.5	"
Supply current (-)	I_{EE}	$R_L = \infty$	-55°C $\leq T_A \leq$125°C	-6.5		"
Common mode rejection ratio (x)	CMRR(x)	-10 V $\leq V_x \leq$+10 V $V_y = \pm 10$ V	-55°C $\leq T_A \leq$125°C	50.0		dB
Common mode rejection ratio (y)	CMRR(y)	-10 V $\leq V_y \leq$+10 V $V_x = \pm 10$ V	T_A = -55°C 25°C $\leq T_A \leq$125°C	"		"

Table 3. (cont.)

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Min	Limits Max	Unit
Common mode rejection ratio (y)	CMRR(y)	-10 V $\leq V_y \leq$ +10 V V_x = +10 V	T_A = -55°C 25°C $\leq T_A \leq$ 125°C	50.0		dB
Output voltage swing	V_{OP}		-55°C $\leq T_A \leq$ 125°C	+10.0		V
					-10.0	
Power supply rejection ratio (-)	PSRR1	15.0 [redacted] V $\leq V_S \leq$ +15 V, V_y = +10 V, V_x = [redacted] V +10V	-55°C $\leq T_A \leq$ 125°C	-10.0	+10.0	mV/V
Power supply rejection ratio (+)	PSRR2	±15 V $\leq V_S \leq$ ±18 V, V_x = [redacted] V, V_y = +10 V +10V	-55°C $\leq T_A \leq$ 125°C	– -50.0	– +50.0	"
Settling time (+)	ts(+)	See figure 5	T_A = 25°C		2.0	µs
Settling time (-)	ts(-)	See figure 5	T_A = 25°C		"	"
Slew rate (+)	SR(+)		-55°C $\leq T_A \leq$ 125°C	25.0		V/µs
Slew rate (-)	SR(-)		-55°C $\leq T_A \leq$ 125°C	35.0		"
Feedthrough (x)	FTx		-55°C $\leq T_A \leq$ 125°C	-100.0	100.0	mV
Feedthrough (y)	FTy		-55°C $\leq T_A \leq$ 125°C	-80.0	80.0	"
Small signal amplitude error (x)	AEx	V_x = 2 V(p-p) Cc = 1000 pF, V_y = +10 V 1% error	T_A 25°C	70.0		kHz
Small signal amplitude error (y)	AEy	V_y = 2 V(p-p) Cc = 1000 pF, V_x = +10 V 1% error	T_A 25°C	"		"
Nonlinearity (x)	NLx		-55°C $\leq T_A \leq$ 125°C	-0.6	0.6	%FS
Nonlinearity (y)	NLy		-55°C $\leq T_A \leq$ 125°C	-0.4	0.4	"
Wideband noise	NI(BB)		T_A = 25°C		3.0	mV rms

Table 3. (cont.)

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Min	Limits Max	Unit
Multiplier accuracy (-x)(-y)	MAx-y-	Vx = -10 V	$T_A = 25°C$	-1.0	1.0	%FS
		Vy = -10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy (-x)(+y)	MAx-y+	Vx = -10 V	$T_A = 25°C$	-1.0	1.0	"
		Vy = +10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy (+x)(-y)	MAx+y-	Vx = +10 V	$T_A = 25°C$	-1.0	1.0	"
		Vy = -10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy (+x)(+y)	MAx+y+	Vx = +10 V	$T_A = 25°C$	-1.0	1.0	"
		Vy = +10 V	$-55°C \leq T_A \leq 125°C$	-4.0	4.0	
Multiplier accuracy drift	$\frac{MA\ xy}{\Delta T}$	Vx = ±10 V Vy = ±10 V	$-55°C \leq T_A \leq 125°C$	-0.04	0.04	$\frac{\%FS}{°C}$
Output offset voltage	V_{OIO}	Vx = Vy = Vz = 0	$T_A = 25°C$	-30.0	30.0	mV
			$T_A = -55°C$	-100.0	100.0	
			$T_A = 125°C$	"	"	
Output offset voltage drift	$\frac{V_{OIO}}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-1.0	1.0	$\frac{mV}{°C}$
Offset voltage (x)	$V_{IO}(x)$		$T_A = 25°C$	-40.0	40.0	mV
			$T_A = -55°C$	-90.0	90.0	
			$T_A = 125°C$	"	"	
Output offset voltage drift (x)	$\frac{V_{OIO}(x)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-800.0	800.0	$\frac{\mu V}{°C}$
Offset voltage (y)	$V_{IO}(y)$		$T_A = 25°C$	-50.0	50.0	mV
			$T_A = -55°C$	-100.0	100.0	
			$T_A = 125°C$	"	"	

Table 3. Electrical Parameter Limits Device Type 04

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Min	Limits Max	Unit
Offset voltage drift (y)	$\frac{V_{IO}(y)}{\Delta T}$		ΔT_A from -55°C to 25°C ΔT_A from 25°C to 125°C	-800.0	800.0	$\frac{\mu V}{°C}$
Input bias current (z)	$I_{IB}(z)$		-55°C $\leq T_A \leq$ 125°C	---	6.0	µA
Input bias current (+)	$+I_{IB}$		T_A = -55°C	-6.0	•	•
			25°C $\leq T_A \leq$125°C	-2.5	2.5	
Input offset current (-)	$-I_{IB}$		T_A = -55°C	-6.0	6.0	•
			25°C $\leq T_A \leq$125°C	-2.5	2.5	
Input offset current	I_{IO}		T_A = 25°C	-200.0	200.0	nA
			-55°C $\leq T_A \leq$125°C	-400.0	400.0	
Output short circuit current (+)	$I_{OS}(+)$	R_L = 0	-55°C $\leq T_A \leq$25°C	-30.0		mA
			T_A = 125°C	•		
Output short circuit current (-)	$I_{OS}(-)$	R_L = 0	-55°C $\leq T_A \leq$25°C		30.0	•
			T_A = 125°C		•	
Supply current (+)	I_{CC}	$R_L = \infty$	-55°C $\leq T_A \leq$125°C		6.0	•
Supply current (-)	I_{EE}	$R_L = \infty$	-55°C $\leq T_A \leq$125°C	-6.0		•
Common mode rejection ratio (x)	CMRR(x)	-6 V $\leq$Vx $\leq$+10 V Vy = $\mp$10 V	-55°C $\leq T_A \leq$125°C	50.0		dB
Common mode rejection ratio (y)	CMRR(y)	-6 V $\leq$Vy $\leq$+10 V Vx = $\mp$10 V	-55°C $\leq T_A \leq$ 125°C	•		•

Table 3. (cont.)

Characteristics	Symbol	Conditions $V_S = \pm 15$ V, $R_L = 2k\Omega$, paragraph 3.4 and figure 4 unless otherwise specified		Limits Min	Limits Max	Unit
Output voltage swing	V_{OP}		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	+10.0		V
					-10.0	
Power supply rejection ratio (-)	PSRR1	±10.0 [redacted] V $\leq V_S \leq \pm 15$ V, $V_y = +10$ V, V_x = [redacted] V +10	$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-10.0	+10.0	mV/V
Power supply rejection ratio (+)	PSRR2	± 15 V $\leq V_S \leq \pm 18$ V, V_x = [redacted] +10, $V_y = +10$ V	$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-40.0	40.0	"
Settling time (+)	ts(+)	See figure 5	$T_A = 25^{\circ}C$		2.0	µs
Settling time (-)	ts(-)	See figure 5	$T_A = 25^{\circ}C$		"	"
Slew rate (+)	SR(+)		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	20.0		V/µs
Slew rate (-)	SR(-)		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	"		"
Feedthrough (x)	FTx		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-50.0	50.0	mV
Feedthrough (y)	FTy		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-40.0	40.0	"
Small signal amplitude error (x)	AEx	$V_x = 2$ V (p-p) $C_c = 1000$ pF, $V_y = +10$ V 1% error	$T_A = 25^{\circ}C$	70.0		kHz
Small signal amplitude error (y)	AEy	$V_y = 2$ V(p-p) $C_c = 1000$ pF, $V_x = +10$ V 1% error	$T_A = 25^{\circ}C$	"		"
Nonlinearity (x)	NLx		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-0.6	0.6	%FS
Nonlinearity (y)	NLy		$-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-0.4	0.4	"
Wideband noise	NI(BB)		$T_A = 25^{\circ}C$		3.0	mV rms

Table 3. (cont)

* * * * * RADC REFERENCE CODE: 0534RK.ARY:OFF
* * SOURCE TEST SPECIFICATION:
* * * * GENERIC TYPE/COMMENT:

PARM NUMB	() DEVICE> / () TEMP> / () FILE>	54 / -55 C / 0	54 / 25 C / 0	54 / 125 C / 0	55 / -55 C / 0	55 / 25 C / 0	55 / 125 C / 0
1	MAXY1(-,-)	10.05 V	10.01 V	9.950 V	10.07 V	10.01 V	9.940 V
2	MAXY1(0,-)	1.050MV	-4.250MV	8.050MV	-11.60MV	650.0UV	19.50MV
3	MAXY1(+,-)	-10.09 V	-9.980 V	*B -10.22 V	-10.11 V	-10.00 V	-9.985 V
4	MAXY1(-,0)	-4.150MV	-1.700MV	20.25MV	-8.300MV	4.550MV	22.45MV
5	OUTOFF	-11.45MV	-7.300MV	16.10MV	-10.45MV	3.000MV	22.35MV
6	MAXY1(+,0)	2.000MV	7.450MV	30.35MV	-9.250MV	3.600MV	23.05MV
7	MAXY1(-,+)	-10.04 V	-10.05 V	-10.08 V	-10.13 V	-10.01 V	-9.895 V
8	MAXY1(0,+)	-22.35MV	-4.750MV	24.30MV	-8.750MV	5.700MV	25.70MV
9	MAXY1(+,+)	10.00 V	9.965 V	9.935 V	10.03 V	9.965 V	9.910 V
10	MAXY2(-,-)	10.02 V	10.00 V	9.955 V	10.05 V	10.00 V	9.985 V
11	MAXY2(0,-)	-27.70MV	-4.750MV	18.55MV	-15.35MV	-900.0UV	19.35MV
12	MAXY2(+,-)	-10.13 V	-10.03 V	-9.900 V	-10.07 V	-10.00 V	-9.880 V
13	MAXY2(-,0)	900.0UV	5.950MV	29.15MV	-11.35MV	1.900MV	21.25MV
14	OUTOFF	-11.70MV	-7.050MV	16.15MV	-10.45MV	2.800MV	22.70MV
15	MAXY2(+,0)	-6.550MV	-250.0UV	22.70MV	-6.150MV	6.700MV	25.30MV
16	MAXY2(-,+)	-10.03 V	*B -10.13 V	-9.840 V	-10.05 V	-10.00 V	-9.805 V
17	MAXY2(0,+)	6.350MV	-3.950MV	15.10MV	-4.350MV	7.550MV	27.15MV
18	MAXY2(+,+)	10.02 V	9.900 V	9.920 V	10.05 V	9.995 V	9.915 V
19	IIBX1	505.0NA	300.0NA	190.0NA	520.0NA	305.0NA	210.0NA
20	IIBX2	500.0NA	285.0NA	180.0NA	540.0NA	310.0NA	220.0NA
21	IIBY1	520.0NA	300.0NA	195.0NA	555.0NA	330.0NA	215.0NA
22	IIBY2	560.0NA	345.0NA	200.0NA	540.0NA	310.0NA	220.0NA
23	IIBZ1	525.0NA	280.0NA	170.0NA	610.0NA	340.0NA	210.0NA
24	IIBZ2	730.0NA	380.0NA	235.0NA	515.0NA	305.0NA	210.0NA
25	OSCP	-25.20MA	-19.10MA	-11.40MA	-27.25MA	-20.80MA	-12.60MA
26	OSCM	*A 34.10MA	27.95MA	20.80MA	*A 36.70MA	*A 30.15MA	22.30MA
27	ISCP	4.065MA	4.155MA	4.350MA	4.235MA	4.400MA	4.750MA
28	ISCM	-4.080MA	-4.190MA	-4.355MA	-4.265MA	-4.470MA	-4.745MA
29	-XCMRR	76.79 DB	84.38 DB	86.18 DB	90.60 DB	87.29 DB	94.52 DB
30	+XCMRR	86.90 DB	110.5 DB	88.43 DB	87.70 DB	84.54 DB	86.69 DB
31	-YCMRR	96.31 DB	94.38 DB	87.72 DB	87.45 DB	88.31 DB	90.66 DB
32	+YCMRR	71.83 DB	73.15 DB	73.02 DB	73.07 DB	72.95 DB	72.53 DB
33	OUTVSP	11.55 V	11.80 V	12.10 V	11.55 V	11.80 V	12.10 V
34	OUTVSM	-11.70 V	-12.05 V	-12.45 V	-11.75 V	-12.05 V	-12.45 V
35	PSRR,15-13	1.073MV/V	786.6UV/V	580.0UV/V	300.0UV/V	153.4UV/V	106.7UV/V
36	PSRR,18-15	1.017MV/V	1.103MV/V	833.4UV/V	483.4UV/V	343.3UV/V	396.6UV/V
37	XOFF	-250.0UV	9.550MV	-7.975MV	11.80MV	-475.0UV	-19.25MV
38	YOFF	16.83MV	11.88MV	-11.05MV	9.975MV	-3.475MV	-22.05MV
39	IIOX	5.000NA	15.00NA	10.00NA	-20.00NA	-5.000NA	0.000 A
40	IIOY	-60.00NA	-45.00NA	-5.000NA	15.00NA	20.00NA	5.000NA
41	IIOZ	-205.0NA	-100.0NA	-65.00NA	95.00NA	35.00NA	0.000 A
42	XFTHRU	8.675MV	10.10MV	9.200MV	1.675MV	1.075MV	400.0UV
43	YFTHRU	800.0UV	300.0UV	75.00UV	275.0UV	175.0UV	250.0UV
44	PINL	2.425MV	-15.12MV	-49.65MV	-20.63MV	-9.100MV	-9.100MV
45	MINL	-9.275MV	12.13MV	-72.77MV	-9.450MV	2.175MV	4.000MV

* * * * * RADC REFERENCE CODE: 0534RK.ARY:OFF
* * SOURCE TEST SPECIFICATION:
* * * * GENERIC TYPE/COMMENT:

Table 4. AD534 Test Data

PARM NUMB	DEVICE>	56	56	56	57	57	57
	TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
	FILE>	0	0	0	0	0	0
1	MAXY1(-,-)	10.08 V	10.01 V	9.915 V	10.03 V	9.985 V	9.910 V
2	MAXY1(0,-)	550.0UV	-4.050MV	-13.05MV	-3.000MV	-7.100MV	-9.600MV
3	MAXY1(+,-)	-10.07 V	-10.00 V	-9.925 V	-10.13 V	-10.03 V	-10.09 V
4	MAXY1(-,0)	6.750MV	650.0UV	-9.600MV	-9.400MV	-13.80MV	-16.25MV
5	OUTOFF	1.950MV	-3.550MV	-12.15MV	-50.00UV	-4.450MV	-5.000MV
6	MAXY1(+,0)	4.200MV	-1.450MV	-9.500MV	-7.300MV	-10.60MV	-10.85MV
7	MAXY1(-,+)	-10.06 V	-10.01 V	-9.935 V	-10.18 V	-10.03 V	-10.09 V
8	MAXY1(0,+)	3.750MV	-2.250MV	-9.750MV	3.850MV	-1.350MV	-1.650MV
9	MAXY1(+,+)	10.05 V	9.985 V	9.885 V	10.03 V	9.985 V	9.915 V
10	MAXY2(-,-)	10.07 V	10.00 V	9.900 V	10.05 V	10.00 V	9.930 V
11	MAXY2(0,-)	-2.950MV	-8.650MV	-16.80MV	-3.500MV	-8.550MV	-8.600MV
12	MAXY2(+,-)	-10.06 V	-10.01 V	-9.920 V	-10.13 V	-9.975 V	-9.930 V
13	MAXY2(-,0)	1.600MV	-3.550MV	-12.20MV	-9.600MV	-13.25MV	-13.75MV
14	OUTOFF	1.750MV	-3.700MV	-12.15MV	-50.00UV	-4.750MV	-5.650MV
15	MAXY2(+,0)	8.800MV	2.750MV	-7.150MV	-6.850MV	-11.60MV	-13.65MV
16	MAXY2(-,+)	-10.09 V	-10.01 V	-9.920 V	-10.13 V	-10.03 V	-9.955 V
17	MAXY2(0,+)	7.650MV	2.700MV	-6.700MV	3.950MV	350.0UV	-1.700MV
18	MAXY2(+,+)	10.06 V	9.990 V	9.885 V	10.01 V	9.955 V	9.800 V
19	IIBX1	485.0NA	280.0NA	180.0NA	545.0NA	325.0NA	215.0NA
20	IIBX2	480.0NA	295.0NA	185.0NA	555.0NA	320.0NA	220.0NA
21	IIBY1	495.0NA	295.0NA	195.0NA	575.0NA	350.0NA	225.0NA
22	IIBY2	495.0NA	295.0NA	190.0NA	555.0NA	320.0NA	210.0NA
23	IIBZ1	490.0NA	300.0NA	195.0NA	540.0NA	315.0NA	205.0NA
24	IIBZ2	490.0NA	295.0NA	190.0NA	560.0NA	330.0NA	215.0NA
25	OSCP	-27.20NA	-20.75NA	-12.60NA	-87.60NA	-81.05NA	[illegible]
26	OSCM	35.25NA	20.90NA	21.70NA	30.10NA	31.05NA	[illegible]
27	ISCP	3.990NA	4.175NA	4.390NA	4.290NA	4.400NA	[illegible]
28	ISCM	-4.005NA	-4.180NA	-4.405NA	-4.305NA	-4.470NA	-4.700NA
29	-XCMRR	92.29 DB	93.39 DB	90.14 DB	86.47 DB	92.51 DB	89.29 DB
30	+XCMRR	87.51 DB	86.16 DB	84.34 DB	83.85 DB	86.21 DB	88.02 DB
31	-YCMRR	86.94 DB	90.37 DB	89.76 DB	80.66 DB	89.74 DB	93.19 DB
32	+YCMRR	73.12 DB	73.12 DB	72.91 DB	72.90 DB	72.90 DB	72.65 DB
33	OUTVSP	11.60 V	11.85 V	12.10 V	11.50 V	11.85 V	12.10 V
34	OUTVSM	-11.75 V	-12.05 V	-12.45 V	-11.70 V	-12.05 V	-12.45 V
35	PSRR,15-13	-1.613MV/V	-1.713MV/V	-1.813MV/V	-359.9UV/V	-279.9UV/V	-493.3UV/V
36	PSRR,18-15	-1.423MV/V	-1.453MV/V	-1.253MV/V	-206.7UV/V	-120.0UV/V	-3.330UV/V
37	XOFF	-350.0UV	4.450MV	14.20MV	3.475MV	7.225MV	9.775MV
38	YOFF	-3.225MV	2.500MV	12.20MV	1.100MV	6.050MV	8.500MV
39	IIOX	5.000NA	-15.00NA	-5.000NA	-10.00NA	5.000NA	-5.000NA
40	IIOY	0.000 A	0.000 A	5.000NA	20.00NA	30.00NA	15.00NA
41	IIOZ	0.000 A	5.000NA	5.000NA	-20.00NA	-15.00NA	-10.00NA
42	XFTHRU	3.525MV	3.150MV	2.600MV	-8.300MV	-7.750MV	-7.750MV
43	YFTHRU	200.0UV	400.0UV	350.0UV	475.0UV	125.0UV	175.0UV
44	PXNL	-4.375MV	-5.125MV	-7.625MV	-39.42MV	-10.48MV	-44.17MV
45	MXNL	975.0UV	4.525MV	4.425MV	-22.25MV	-7.700MV	-41.45MV

= = = = = RADC REFERENCE CODE: 0534RN.ARY1OFF
= = SOURCE TEST SPECIFICATION:
= = = = GENERIC TYPE/COMMENT:

PARM NUMB	DEVICE>	58	58	58	59	59	59
	TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
	FILE>	0	0	0	0	0	0
1	MAXY1(-,-)	10.05 V	10.00 V	9.930 V	10.03 V	9.990 V	9.925 V
2	MAXY1(0,-)	-25.75MV	-19.85MV	-9.950MV	-16.80MV	-10.85MV	-10.10MV
3	MAXY1(+,-)	-10.15 V	-10.09 V	-10.09 V	-10.11 V	-10.03 V	-9.920 V

Table 4. (cont.)

4 MAXY1(-,0)	-24.50MV	-18.10MV	-7.350MV	-18.15MV	-14.40MV	-11.35MV
5 OUTOFF	-24.35MV	-16.35MV	-3.750MV	-15.10MV	-9.100MV	-6.000MV
6 MAXY1(+,0)	-21.75MV	-14.25MV	-2.850MV	-11.80MV	-6.400MV	-5.300MV
7 MAXY1(-,+)	-10.13 V	*B -10.13 V	-9.965 V	-10.10 V	-10.03 V	-9.920 V
8 MAXY1(0,+)	-22.65MV	-12.05MV	3.600MV	-12.55MV	-6.600MV	-1.000MV
9 MAXY1(+,+)	10.01 V	9.965 V	9.895 V	10.02 V	9.985 V	9.925 V
10 MAXY2(-,-)	10.02 V	9.980 V	9.905 V	10.03 V	10.00 V	9.940 V
11 MAXY2(0,-)	-30.15MV	-19.95MV	-4.250MV	-20.50MV	-14.65MV	-9.200MV
12 MAXY2(+,-)	-10.06 V	*B -10.13 V	-9.970 V	-10.13 V	-10.03 V	-9.915 V
13 MAXY2(-,0)	-24.15MV	-17.05MV	-4.800MV	-14.40MV	-10.95MV	-7.800MV
14 OUTOFF	-24.25MV	-16.10MV	-3.250MV	-15.00MV	-9.100MV	-6.000MV
15 MAXY2(+,0)	-21.55MV	-15.20MV	-4.450MV	-14.95MV	-11.10MV	-8.000MV
16 MAXY2(-,+)	-10.13 V	*B -10.13 V	-9.900 V	-10.18 V	*B -10.13 V	-10.09 V
17 MAXY2(0,+)	-18.15MV	-11.95MV	-1.650MV	-8.850MV	-2.900MV	-1.850MV
18 MAXY2(+,+)	10.03 V	9.985 V	9.905 V	10.00 V	9.970 V	9.900 V
19 IIBX1	515.0NA	300.0NA	200.0NA	435.0NA	250.0NA	160.0NA
20 IIBX2	545.0NA	320.0NA	210.0NA	440.0NA	260.0NA	165.0NA
21 IIBY1	555.0NA	320.0NA	210.0NA	490.0NA	275.0NA	185.0NA
22 IIBY2	535.0NA	315.0NA	220.0NA	460.0NA	265.0NA	175.0NA
23 IIBZ1	520.0NA	300.0NA	200.0NA	450.0NA	255.0NA	170.0NA
24 IIBZ2	735.0NA	400.0NA	395.0NA	455.0NA	250.0NA	155.0NA
25 OSCP	-28.00MA	-21.40MA	-13.20MA	-26.65MA	-20.05MA	-12.20MA
26 OSCM	*A 39.10MA	*A 31.85MA	24.05MA	*A 37.35MA	*A 30.40MA	22.05MA
27 ISCP	4.190MA	4.410MA	4.635MA	4.075MA	4.270MA	4.520MA
28 ISCM	-4.195MA	-4.400MA	-4.600MA	-4.110MA	-4.295MA	-4.520MA
29 -XCMRR	90.12 DB	86.76 DB	80.69 DB	86.09 DB	80.36 DB	80.31 DB
30 +XCMRR	87.07 DB	83.41 DB	83.54 DB	84.32 DB	83.22 DB	83.89 DB
31 -YCMRR	87.15 DB	88.11 DB	80.25 DB	87.41 DB	89.19 DB	89.40 DB
32 +YCMRR	73.05 DB	72.99 DB	72.99 DB	72.96 DB	73.03 DB	73.40 DB
33 OUTVSP	11.60 V	11.85 V	12.15 V	11.60 V	11.85 V	12.15 V
34 OUTVSM	-11.75 V	-12.10 V	-12.50 V	-11.80 V	-12.10 V	-12.40 V
35 PSRR,15-13	-340.0UV/V	-246.7UV/V	-333.3UV/V	-433.3UV/V	-413.4UV/V	-560.0UV/V
36 PSRR,18-15	-140.0UV/V	-93.30UV/V	-26.70UV/V	-60.00UV/V	-200.0UV/V	-270.0UV/V
37 XOFF	25.90MV	*A 20.25MV	10.53MV	17.22MV	11.22MV	10.55MV
38 YOFF	25.73MV	18.27MV	6.000MV	18.27MV	12.10MV	9.025MV
39 IIOX	-30.00NA	-20.00NA	-10.00NA	-5.000NA	-10.00NA	-5.000NA
40 IIOY	20.00NA	5.000NA	-10.00NA	30.00NA	10.00NA	10.00NA
41 IIOZ	-215.0NA	-180.0NA	-155.0NA	-5.000NA	5.000NA	15.00NA
42 XFTHRU	1.225MV	175.0UV	-4.350MV	125.0UV	-3.300MV	-3.325MV
43 YFTHRU	150.0UV	400.0UV	575.0UV	425.0UV	375.0UV	450.0UV
44 PXNL	-18.67MV	-33.97MV	-24.30MV	-13.72MV	-7.950MV	1.750MV
45 MXNL	-10.86MV	-11.33MV	-36.27MV	-11.60MV	-4.575MV	6.300MV

= = = = = QAGC REFERENCE CODE: DS34RK.ARY1OFF
= = SOURCE TEST SPECIFICATION:
= = = = GENERIC TYPE/COMMENT:

PARM () DEVICE>	60	60	60	61	61	61
NUMB () TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
() FILE>	0	0	0	0	0	0
1 MAXY1(-,-)	10.86 V	10.00 V	9.916 V	9.805 V	9.900 V	10.03 V
2 MAXY1(0,-)	-9.750MV	-8.200MV	-3.000MV	-13.10MV	-15.55MV	-13.95MV
3 MAXY1(+,-)	-10.04 V	-9.920 V	-9.905 V	-10.05 V	-10.03 V	-10.10 V
4 MAXY1(-,0)	-17.20MV	-9.650MV	-3.400MV	-18.60MV	-6.300MV	-3.300MV
5 OUTOFF	-11.20MV	-7.600MV	-1.150MV	-10.65MV	-12.95MV	-12.15MV
6 MAXY1(+,0)	-8.350MV	-6.900MV	-200.0UV	14.50MV	-1.300MV	-8.450MV
7 MAXY1(-,+)	-10.18 V	-10.03 V	-9.925 V	-10.10 V	*B -10.13 V	*B -10.22 V
8 MAXY1(0,+)	-11.70MV	-6.100MV	750.0UV	-10.80MV	-11.45MV	-9.300MV
9 MAXY1(+,+)	10.05 V	9.975 V	9.885 V	9.940 V	10.00 V	10.05 V

Table 4. (cont.)

10 MAXY2(-,-)	10.06 V	9.990 V	9.900 V	9.955 V	10.01 V	10.05 V
11 MAXY2(0,-)	-19.75MV	-14.05MV	-5.900MV	-17.95MV	-17.70MV	-16.60MV
12 MAXY2(+,-)	-10.13 V	-10.01 V	-9.905 V	-10.10 V	-10.03 V	-10.07 V
13 MAXY2(-,0)	-5.000MV	-7.800MV	-2.850MV	11.30MV	-4.100MV	-4.750MV
14 OUTOFF	-11.25MV	-7.600MV	-1.100MV	-10.90MV	-13.20MV	-12.25MV
15 MAXY2(+,0)	-14.50MV	-6.500MV	-800.0UV	-15.80MV	-4.200MV	-500.0UV
16 MAXY2(-,+)	-10.13 V	-10.09 V	-9.940 V	-10.05 V	*B -10.13 V	-10.10 V
17 MAXY2(0,+)	-2.050MV	-650.0UV	4.900MV	-6.150MV	-4.400MV	-6.300MV
18 MAXY2(+,+)	10.04 V	9.980 V	9.880 V	9.870 V	9.970 V	10.02 V
19 IIBX1	440.0NA	250.0NA	165.0NA	1.480UA	815.0NA	530.0NA
20 IIBX2	440.0NA	250.0NA	165.0NA	1.220UA	725.0NA	510.0NA
21 IIBY1	475.0NA	275.0NA	190.0NA	1.375UA	795.0NA	520.0NA
22 IIBY2	515.0NA	270.0NA	185.0NA	1.455UA	795.0NA	535.0NA
23 IIBZ1	445.0NA	250.0NA	175.0NA	1.215UA	725.0NA	490.0NA
24 IIBZ2	440.0NA	255.0NA	170.0NA	1.255UA	740.0NA	495.0NA
25 OSCP	-27.40MA	-20.75MA	-12.55MA	*B -30.65MA	-24.25MA	-15.90MA
26 OSCM	*A 36.35MA	29.55MA	22.15MA	*A 38.50MA	*A 32.00MA	24.85MA
27 ISCP	4.285MA	4.455MA	4.750MA	4.180MA	4.300MA	6.395MA
28 ISCM	-4.310MA	-4.510MA	-4.765MA	-4.190MA	-4.330MA	-4.455MA
29 -XCHRR	86.82 DB	87.60 DB	93.27 DB	101.5 DB	87.38 DB	87.37 DB
30 +XCHRR	83.58 DB	85.85 DB	87.05 DB	80.29 DB	83.85 DB	82.77 DB
31 -YCHRR	82.34 DB	86.76 DB	92.51 DB	87.11 DB	87.85 DB	89.53 DB
32 +YCHRR	73.07 DB	73.07 DB	72.90 DB	72.36 DB	72.86 DB	72.74 DB
33 OUTVSP	11.55 V	11.80 V	12.10 V	11.65 V	11.95 V	12.25 V
34 OUTVSM	-11.70 V	-12.05 V	-12.45 V	-11.75 V	-12.10 V	-12.50 V
35 PSRR,15-13	-440.0UV/V	-466.5UV/V	-373.4UV/V	-246.7UV/V	-320.1UV/V	-500.0UV/V
36 PSRR,18-15	-333.3UV/V	-183.3UV/V	-350.0UV/V	-66.66UV/V	-216.6UV/V	-186.7UV/V
37 XOFF	10.23MV	8.650MV	3.625MV	11.80MV	15.80MV	16.07MV
38 YOFF	10.62MV	9.975MV	2.750MV	27.20MV	15.45MV	12.47MV
39 IIOX	0.000 A	0.000 A	0.000 A	200.0NA	90.00NA	20.00NA
40 IIOY	-40.00NA	5.000NA	5.000NA	-60.00NA	0.000 A	-15.00NA
41 IIOZ	5.000NA	-5.000NA	5.000NA	-40.00NA	-15.00NA	-5.000NA
42 XFTHRU	1.425MV	325.0UV	-650.0UV	8.600MV	9.150MV	9.175MV
43 YFTHRU	475.0UV	450.0UV	25.00UV	-1.300MV	-550.0UV	525.0UV
44 PXNL	-29.15MV	-10.70MV	-10.37MV	-35.65MV	-26.78MV	-40.35MV
45 MXNL	9.875MV	24.10MV	2.750MV	-34.70MV	-4.725MV	-9.275MV

* * * * * RADC REFERENCE CODE: 0534RK.ARY:OFF
* * SOURCE TEST SPECIFICATION:
* * * * GENERIC TYPE/COMMENT:

PARM [] DEVICE>	62	62	62	63	63	63
NUMB [] TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
[] FILE>	0	0	0	0	0	0
1 MAXY1(-,-)	10.04 V	10.01 V	9.945 V	10.07 V	10.01 V	9.925 V
2 MAXY1(0,-)	-6.700MV	-1.500MV	6.500MV	-250.0UV	-2.400MV	-4.000MV
3 MAXY1(+,-)	-10.03 V	-10.01 V	-9.925 V	-10.07 V	-10.03 V	-9.925 V
4 MAXY1(-,0)	-12.05MV	-6.600MV	4.400MV	-400.0UV	-3.050MV	-5.300MV
5 OUTOFF	-6.650MV	-2.050MV	6.650MV	-1.350MV	-3.100MV	-3.700MV
6 MAXY1(+,0)	-3.900MV	1.200MV	9.050MV	-1.600MV	-4.350MV	-4.950MV
7 MAXY1(-,+)	-10.05 V	-10.02 V	-9.940 V	-10.18 V	*B -10.13 V	-9.935 V
8 MAXY1(0,+)	-6.350MV	-2.250MV	7.350MV	-2.000MV	-3.050MV	-2.450MV
9 MAXY1(+,+)	10.02 V	9.985 V	9.920 V	10.03 V	9.980 V	9.890 V
10 MAXY2(-,-)	10.04 V	10.00 V	9.935 V	10.05 V	9.990 V	9.905 V
11 MAXY2(0,-)	-19.75MV	-9.350MV	-850.0UV	-6.850MV	-10.30MV	-10.40MV
12 MAXY2(+,-)	-10.03 V	-10.02 V	-9.930 V	-10.05 V	-10.01 V	-9.925 V
13 MAXY2(-,0)	-6.400MV	-1.250MV	6.050MV	-4.150MV	-6.750MV	-7.650MV
14 OUTOFF	-6.050MV	-2.200MV	6.800MV	-1.550MV	-3.100MV	-3.900MV
15 MAXY2(+,0)	-9.200MV	-2.050MV	7.150MV	1.800MV	-450.0UV	-2.150MV

Table 4. (cont.)

16	MAXY2(-,+)	-10.13 V	-9.920 V	-9.920 V	-10.04 V	-10.05 V	-9.985 V
17	MAXY2(0,+)	-1.050MV	5.900MV	15.00MV	6.900MV	4.900MV	3.700MV
18	MAXY2(+,+)	10.02 V	9.990 V	9.925 V	10.05 V	9.990 V	9.900 V
19	IIBX1	770.0NA	480.0NA	320.0NA	505.0NA	290.0NA	190.0NA
20	IIBX2	735.0NA	440.0NA	300.0NA	510.0NA	295.0NA	200.0NA
21	IIBY1	755.0NA	455.0NA	315.0NA	530.0NA	305.0NA	200.0NA
22	IIBY2	735.0NA	450.0NA	315.0NA	515.0NA	315.0NA	205.0NA
23	IIBZ1	785.0NA	480.0NA	315.0NA	510.0NA	290.0NA	210.0NA
24	IIBZ2	775.0NA	465.0NA	315.0NA	505.0NA	290.0NA	195.0NA
25	OSCP	*A -30.45MA	-23.65MA	-15.05MA	-27.35MA	-20.95MA	-12.90MA
26	OSCM	*A 37.90MA	*A 31.25MA	23.95MA	*A 30.20MA	29.65MA	22.30MA
27	ISCP	4.325MA	4.505MA	4.785MA	4.205MA	4.395MA	4.655MA
28	ISCM	-4.365MA	-4.565MA	-4.805MA	-4.235MA	-4.400MA	-4.660MA
29	-XCMRR	96.23 DB	90.96 DB	90.54 DB	90.29 DB	90.17 DB	93.19 DB
30	+XCMRR	87.29 DB	87.66 DB	86.56 DB	86.07 DB	85.32 DB	86.16 DB
31	-YCMRR	86.02 DB	85.47 DB	85.40 DB	87.03 DB	87.45 DB	89.45 DB
32	+YCMRR	73.19 DB	73.18 DB	73.11 DB	73.03 DB	72.85 DB	72.77 DB
33	OUTVSP	11.55 V	11.80 V	12.10 V	11.60 V	11.85 V	12.10 V
34	OUTVSM	-11.70 V	-12.05 V	-12.40 V	-11.75 V	-12.05 V	-12.45 V
35	PSRR,15-13	-526.7UV/V	-513.4UV/V	-573.3UV/V	-466.7UV/V	-540.1UV/V	-606.7UV/V
36	PSRR,18-15	-216.6UV/V	-166.7UV/V	-210.0UV/V	-340.0UV/V	-463.3UV/V	-380.0UV/V
37	XOFF	8.825MV	1.675MV	-6.225MV	475.0UV	2.775MV	4.475MV
38	YOFF	12.73MV	4.950MV	-4.325MV	750.0UV	2.350MV	3.875MV
39	IIOX	35.00NA	40.00NA	20.00NA	-5.000NA	-5.000NA	-10.00NA
40	IIOY	20.00NA	5.000NA	0.000 A	15.00NA	-10.00NA	-5.000NA
41	IIOZ	10.00NA	15.00NA	0.000 A	5.000NA	0.000 A	15.00NA
42	XFTHRU	675.0UV	350.0UV	75.00UV	350.0UV	-700.0UV	-1.425MV
43	YFTHRU	125.0UV	175.0UV	275.0UV	225.0UV	375.0UV	[illegible]
44	PXNL	-3.325MV	-7.625MV	-6.675MV	-36.50MV	-34.75MV	[illegible]
45	MXNL	5.600MV	750.0UV	1.750MV	-2.375MV	-3.800MV	2.000MV

Table 4. (cont.)

R A D C STANDARD LIMIT SET SUMMARY

LIMSIM PROGRAM SUMMARY LISTING
  * PRECEDING A LIMIT VALUE INDICATES A LIMIT NOT REQUIRED BY SPEC
    THIS IS AN EXTENDED LIMIT IMPOSED BY RADC T/E

REFERENCE DISK ARRAY=D534RH.ARY1OFF

SOURCE TEST SPEC=

GENERIC TYPE=

TXN/PARAMETER	MIN @ 25C	MAX @ 25C	DELTA LIMIT	MIN @ -55C	MAX @ -55C	DELTA LIMIT	MIN @ 125C	MAX @ 125C	DELTA LIMIT
1 MAXY1(-,-)	9.900 V	10.10 V	-----	9.800 V	10.20 V	-----	9.800 V	10.20 V	-----
2 MAXY1(0,-)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
3 MAXY1(+,-)	-10.10 V	-9.900 V	-----	-10.20 V	-9.800 V	-----	-10.20 V	-9.800 V	-----
4 MAXY1(-,0)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
5 OUTOFF	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
6 MAXY1(+,0)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
7 MAXY1(-,+)	-10.10 V	-9.900 V	-----	-10.20 V	-9.800 V	-----	-10.20 V	-9.800 V	-----
8 MAXY1(0,+)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
9 MAXY1(+,+)	9.900 V	10.10 V	-----	9.800 V	10.20 V	-----	9.800 V	10.20 V	-----
10 MAXY2(-,-)	9.900 V	10.10 V	-----	9.800 V	10.20 V	-----	9.800 V	10.20 V	-----
11 MAXY2(0,-)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
12 MAXY2(+,-)	-10.10 V	-9.900 V	-----	-10.20 V	-9.800 V	-----	-10.20 V	-9.800 V	-----
13 MAXY2(-,0)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
14 OUTOFF	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
15 MAXY2(+,0)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
16 MAXY2(-,+)	-10.10 V	-9.900 V	-----	-10.20 V	-9.800 V	-----	-10.20 V	-9.800 V	-----
17 MAXY2(0,+)	-100.0MV	100.0MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----
18 MAXY2(+,+)	9.900 V	10.10 V	-----	9.800 V	10.20 V	-----	9.800 V	10.20 V	-----
19 IIBX1	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----
20 IIBX2	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----
21 IIBY1	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----
22 IIBY2	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----
23 IIBZ1	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----
24 IIBZ2	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----	0.000 A	2.000UA	-----
25 USCP	-30.00MA	0.000 A	-----	-30.00MA	0.000 A	-----	-30.00MA	0.000 A	-----
26 DSCM	0.000 A	30.00MA	-----	0.000 A	30.00MA	-----	0.000 A	30.00MA	-----
27 ISCP	0.000 A	6.000MA	-----	0.000 A	6.000MA	-----	0.000 A	6.000MA	-----
28 ISCM	-6.000MA	0.000 A	-----	-6.000MA	0.000 A	-----	-6.000MA	0.000 A	-----
29 -XCMRR	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----
30 +XCMRR	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----
31 -YCMRR	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----
32 +YCMRR	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----	60.00 DB	* 120.0 DB	-----
33 OUTVSP	11.00 V	* 20.00 V	-----	11.00 V	* 20.00 V	-----	11.00 V	* 20.00 V	-----
34 OUTVSM	-20.00 V	* -11.00 V	-----	-20.00 V	* -11.00 V	-----	-20.00 V	* -11.00 V	-----
35 PSRR,15-13	-10.00MV/V	10.00MV/V	-----	-10.00MV/V	10.00MV/V	-----	-10.00MV/V	10.00MV/V	-----
36 PSRR,18-15	-4.000MV/V	4.000MV/V	-----	-4.000MV/V	4.000MV/V	-----	-4.000MV/V	4.000MV/V	-----
37 XOFF	-20.00MV	20.00MV	-----	-45.00MV	45.00MV	-----	-45.00MV	45.00MV	-----
38 YOFF	-20.00MV	20.00MV	-----	-45.00MV	45.00MV	-----	-45.00MV	45.00MV	-----
39 IIOX	-250.0NA	250.0NA	-----	-300.0NA	300.0NA	-----	-250.0NA	250.0NA	-----
40 IIOY	-250.0NA	250.0NA	-----	-300.0NA	300.0NA	-----	-250.0NA	250.0NA	-----
41 IIOZ	-250.0NA	250.0NA	-----	-300.0NA	300.0NA	-----	-250.0NA	250.0NA	-----
42 XFTHRU	-60.00MV	60.00MV	-----	-70.00MV	70.00MV	-----	-70.00MV	70.00MV	-----

Table 4. (cont.)

43 VFTHRU	I -20.00MV	20.00MV	I	-----	I -24.00MV	24.00MV	I	-----	I -24.00MV	24.00MV	I	----- I
44 PXNL	I -60.00MV	60.00MV	I	-----	I -150.0MV	150.0MV	I	-----	I -150.0MV	150.0MV	I	----- I
45 MXNL	I -60.00MV	60.00MV	I	-----	I -150.0MV	150.0MV	I	-----	I -150.0MV	150.0MV	I	----- I

Table 4. (cont.)

* * * * * RADC REFERENCE CODE: 0532RL.ARY1OFF
* * SOURCE TEST SPECIFICATION:
* * * * GENERIC TYPE/COMMENT:

PARM ()	DEVICE>	1176	1176	1176	1177	1177	1177
NUMB ()	TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
()	FILE>	0	0	0	0	0	0
1	MAXY1(-,-)	10.05 V	10.06 V	10.11 V	10.03 V	10.05 V	10.08 V
2	MAXY1(0,-)	-90.45MV	-60.60MV	-60.75MV	46.55MV	41.55MV	18.20MV
3	MAXY1(+,-)	-10.06 V	*B -10.10 V	-10.16 V	-9.950 V	-9.975 V	-10.07 V
4	MAXY1(-,0)	-26.90MV	-24.45MV	-32.65MV	68.60MV	43.80MV	28.50MV
5	OUTOFF	-90.00MV	-75.00MV	-74.00MV	29.00MV	20.60MV	14.75MV
6	MAXY1(+,0)	-29.95MV	-25.75MV	-23.00MV	50.15MV	51.50MV	42.15MV
7	MAXY1(-,+)	-10.12 V	*B -10.13 V	-10.20 V	-9.945 V	-9.905 V	-10.06 V
8	MAXY1(0,+)	-94.00MV	-74.50MV	-71.50MV	22.65MV	29.60MV	25.20MV
9	MAXY1(+,+)	9.905 V	10.00 V	10.07 V	10.00 V	10.03 V	10.08 V
10	MAXY2(-,-)	10.00 V	10.03 V	10.10 V	10.02 V	10.05 V	10.11 V
11	MAXY2(0,-)	-102.5MV	-62.00MV	-80.00MV	14.15MV	20.30MV	16.00MV
12	MAXY2(+,-)	-10.09 V	*B -10.10 V	-10.18 V	-9.930 V	-9.955 V	-10.02 V
13	MAXY2(-,0)	-40.00MV	-33.75MV	-33.00MV	39.00MV	38.40MV	30.30MV
14	OUTOFF	-79.50MV	-74.50MV	-72.00MV	29.65MV	26.75MV	16.10MV
15	MAXY2(+,0)	-4.800MV	-10.00MV	-8.800MV	70.00MV	64.60MV	56.25MV
16	MAXY2(-,+)	-10.12 V	*B -10.14 V	-10.21 V	-9.900 V	-10.02 V	-10.10 V
17	MAXY2(0,+)	-75.50MV	-79.50MV	-73.00MV	33.60MV	22.20MV	5.400MV
18	MAXY2(+,+)	10.02 V	10.02 V	10.00 V	10.00 V	10.01 V	10.05 V
19	IIBX1	815.0NA	550.0NA	395.0NA	555.0NA	450.0NA	225.0NA
20	IIBX2	760.0NA	490.0NA	330.0NA	535.0NA	495.0NA	285.0NA
21	IIBY1	795.0NA	525.0NA	355.0NA	610.0NA	440.0NA	200.0NA
22	IIBY2	875.0NA	570.0NA	360.0NA	540.0NA	420.0NA	215.0NA
23	IIBZ1	9.450UA	8.450UA	8.200UA	6.750UA	7.150UA	6.900UA
24	OSCP	-25.25MA	-19.70MA	-12.75MA	*B -31.60MA	-24.70MA	-16.10MA
25	OSCM	20.90MA	20.10MA	18.95MA	21.35MA	20.50MA	19.10MA
26	ISCP	3.645MA	3.945MA	4.420MA	3.645MA	3.920MA	4.480MA
27	ISCM	-3.705MA	-3.920MA	-4.400MA	-3.660MA	-3.925MA	-4.470MA
28	-XCMRR	67.95 DB	66.41 DB	65.45 DB	66.60 DB	66.32 DB	63.80 DB
29	+XCMRR	65.62 DB	65.05 DB	63.67 DB	65.04 DB	64.97 DB	62.67 DB
30	-YCMRR	74.86 DB	72.56 DB	73.50 DB	73.68 DB	85.43 DB	79.91 DB
31	+YCMRR	83.82 DB	94.33 DB	84.39 DB	86.96 DB	82.46 DB	80.42 DB
32	OUTVSP	11.35 V	11.45 V	11.40 V	11.55 V	11.45 V	11.80 V
33	OUTVSM	-11.00 V	-11.90 V	-11.60 V	-11.50 V	-11.20 V	-11.00 V
34	PSRR,15-13	16.58MV/V	-4.833MV/V	-12.76MV/V	21.79MV/V	4.373MV/V	-10.90MV/V
35	PSRR,18-15	-12.22MV/V	-13.21MV/V	-13.74MV/V	-11.16MV/V	*B -139.5MV/V	-12.96MV/V
36	XOFF	63.23MV	*A 60.05MV	60.63MV	-40.95MV	-34.37MV	-11.25MV
37	YOFF	79.40MV	*A 76.35MV	78.93MV	-20.23MV	-24.75MV	-7.925MV
38	IIOX	55.00NA	60.00NA	65.00NA	20.00NA	-5.000NA	0.000 A
39	IIOY	-40.00NA	-45.00NA	-25.00NA	70.00NA	25.00NA	30.00NA
40	XFTHRU	50.58MV	47.90MV	66.00MV	20.36MV	19.05MV	20.37MV
41	YFTHRU	2.775MV	7.450MV	7.875MV	5.660MV	6.975MV	6.950MV
42	PINL	14.50MV	6.000MV	3.250MV	2.425MV	-3.550MV	-7.660MV
43	MINL	22.72MV	19.05MV	16.62MV	-2.025MV	-3.275MV	-5.350MV

* * * * * RADC REFERENCE CODE: 0532RL.ARY1OFF
* * SOURCE TEST SPECIFICATION:
* * * * GENERIC TYPE/COMMENT:

PARM ()	DEVICE>	1178	1178	1178	1179	1179	1179
NUMB ()	TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C

Table 4. AD532 Test Data (cont.)

()	FILE>	0	0	0	0	0	0
1	MAXY1(-,-)	9.955 V	9.995 V	10.13 V	9.945 V	9.960 V	9.995 V
2	MAXY1(0,-)	-31.05MV	-10.45MV	56.60MV	7.300MV	-10.85MV	-56.65MV
3	MAXY1(+,-)	-10.00 V	-10.01 V	-10.03 V	-9.935 V	-9.995 V	-10.12 V
4	MAXY1(-,0)	-69.00MV	-38.75MV	21.90MV	-1.400MV	-20.95MV	-58.85MV
5	OUTOFF	-45.15MV	-13.35MV	49.40MV	12.60MV	-7.850MV	-48.65MV
6	MAXY1(+,0)	-49.20MV	-14.35MV	47.90MV	6.350MV	-12.05MV	-48.35MV
7	MAXY1(-,+)	-10.08 V	-10.07 V	-10.11 V	-9.960 V	-10.02 V	-10.15 V
8	MAXY1(0,+)	-40.00MV	-1.050MV	54.35MV	28.20MV	8.200MV	-24.80MV
9	MAXY1(+,+)	9.240 V	9.950 V	10.07 V	9.905 V	9.925 V	9.970 V
10	MAXY2(-,-)	9.910 V	9.975 V	10.11 V	9.920 V	9.930 V	9.985 V
11	MAXY2(0,-)	-47.50MV	-10.15MV	45.55MV	19.60MV	-1.650MV	-36.35MV
12	MAXY2(+,-)	-10.07 V	-10.05 V	-10.08 V	-9.945 V	-10.00 V	-10.13 V
13	MAXY2(-,0)	-61.35MV	-25.90MV	36.50MV	-5.250MV	-24.00MV	-59.55MV
14	OUTOFF	-45.05MV	-12.30MV	50.45MV	13.40MV	-7.850MV	-46.00MV
15	MAXY2(+,0)	-49.60MV	-17.50MV	45.55MV	19.75MV	2.000MV	-31.90MV
16	MAXY2(-,+)	-10.03 V	-10.05 V	-10.07 V	-9.960 V	-10.02 V	-10.16 V
17	MAXY2(0,+)	-41.20MV	-20.40MV	45.70MV	-2.800MV	-24.65MV	-69.00MV
18	MAXY2(+,+)	9.915 V	9.965 V	10.10 V	9.930 V	9.935 V	9.980 V
19	IIBX1	1.605UA	945.0NA	630.0NA	920.0NA	590.0NA	430.0NA
20	IIBX2	1.180UA	785.0NA	565.0NA	900.0NA	575.0NA	410.0NA
21	IIBY1	1.300UA	825.0NA	575.0NA	915.0NA	585.0NA	420.0NA
22	IIBY2	1.365UA	900.0NA	635.0NA	910.0NA	585.0NA	480.0NA
23	IIBZ1	4.000UA	3.900UA	3.950UA	5.550UA	5.400UA	5.350UA
24	OSCP	-27.50MA	-21.05MA	-13.30MA	-29.65MA	-23.35MA	-15.95MA
25	OSCM	15.45MA	15.05MA	14.45MA	21.45MA	20.40MA	19.10MA
26	ISCP	3.130MA	3.370MA	3.730MA	3.610MA	3.880MA	4.280MA
27	ISCM	-3.175MA	-3.425MA	-3.745MA	-3.630MA	-3.860MA	-4.295MA
28	-XCMRR	66.48 DB	67.29 DB	66.22 DB	67.03 DB	65.89 DB	[illegible] DB
29	+XCMRR	69.41 DB	66.63 DB	68.06 DB	68.36 DB	64.41 DB	[illegible] DB
30	-YCMRR	76.39 DB	75.66 DB	75.46 DB	74.46 DB	75.03 DB	[illegible] DB
31	+YCMRR	82.11 DB	81.96 DB	80.50 DB	82.46 DB	87.17 DB	79.79 DB
32	OUTVSP	10.45 V	10.70 V	10.90 V	11.20 V	11.25 V	12.35 V
33	OUTVSM	-11.30 V	-10.85 V	-10.75 V	-11.75 V	-11.25 V	-12.00 V
34	PSRR,15-13	7.427MV/V	-16.81MV/V	-22.35MV/V	4.647MV/V	-14.93MV/V	-22.45MV/V
35	PSRR,16-15	-18.54MV/V	-20.06MV/V	-21.43MV/V	-22.06MV/V	-28.63MV/V	-23.00MV/V
36	XOFF	40.60MV	18.05MV	-50.52MV	-8.150MV	17.37MV	64.50MV
37	YOFF	55.05MV	25.55MV	-36.40MV	-4.525MV	12.30MV	53.90MV
38	IIOX	425.0NA	160.0NA	65.00NA	20.00NA	15.00NA	20.00NA
39	IIOY	-65.00NA	-75.00NA	-60.00NA	5.000NA	0.000 A	0.000 A
40	XFTHRU	-13.95MV	-13.20MV	-14.50MV	-10.33MV	-6.650MV	-4.950MV
41	YFTHRU	9.625MV	7.600MV	6.075MV	5.150MV	6.525MV	7.925MV
42	PXNL	-31.25MV	-30.72MV	-35.92MV	-27.85MV	-29.10MV	-32.60MV
43	MXNL	3.025MV	225.1UV	-3.300MV	-1.150MV	-3.325MV	-2.925MV

* * * * * RADC REFERENCE CODE: 0532RL.ARY:OFF
* * SOURCE TEST SPECIFICATIONS
* * * * GENERIC TYPE/COMMENTS

PARM ()	DEVICE>	1180	1180	1180	1181	1181	1181
NUMB ()	TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
()	FILE>	0	0	0	0	0	0
1	MAXY1(-,-)	9.990 V	10.00 V	10.12 V	10.02 V	10.03 V	10.18 V
2	MAXY1(0,-)	-38.30MV	1.000MV	28.75MV	18.15MV	30.30MV	60.50MV
3	MAXY1(+,-)	-10.07 V	-10.03 V	-10.09 V	-10.00 V	-10.02 V	-10.20 V
4	MAXY1(-,0)	-16.25MV	-24.80MV	-50.00UV	-33.55MV	-12.85MV	17.95MV
5	OUTOFF	-23.60MV	-2.000MV	20.25MV	3.000MV	16.40MV	47.60MV
6	MAXY1(+,0)	-60.00MV	-16.25MV	27.15MV	-6.950MV	-4.000MV	17.75MV
7	MAXY1(-,+)	-10.01 V	-10.07 V	-10.15 V	-10.07 V	-10.08 V	-10.18 V

Table 4. (cont.)

8 MAXY1(0,+)	-2.650MV	6.250MV	38.40MV	10.35MV	18.95MV	39.65MV
9 MAXY1(+,+)	9.850 V	9.985 V	10.08 V	9.950 V	9.960 V	10.08 V
10 MAXY2(-,-)	9.875 V	9.965 V	10.11 V	9.985 V	9.980 V	10.10 V
11 MAXY2(0,-)	-10.90MV	-2.000MV	29.40MV	1.300MV	8.750MV	28.00MV
12 MAXY2(+,-)	-9.945 V	-10.05 V	-10.12 V	-10.06 V	-10.05 V	-10.15 V
13 MAXY2(-,0)	-41.00MV	-26.45MV	17.00MV	-16.20MV	-17.55MV	5.200MV
14 OUTOFF	-24.65MV	-250.0UV	31.25MV	3.300MV	14.70MV	40.50MV
15 MAXY2(+,0)	4.050MV	-1.750MV	27.15MV	-13.10MV	8.300MV	43.25MV
16 MAXY2(-,+)	-10.09 V	-10.07 V	-10.13 V	-10.03 V	-10.05 V	-10.15 V
17 MAXY2(0,+)	-48.50MV	-8.450MV	21.00MV	8.450MV	14.95MV	56.50MV
18 MAXY2(+,+)	9.950 V	9.985 V	10.10 V	9.985 V	10.01 V	10.15 V
19 IIBX1	920.0NA	530.0NA	365.0NA	1.915UA	1.070UA	535.0NA
20 IIBX2	1.030UA	585.0NA	355.0NA	1.205UA	760.0NA	390.0NA
21 IIBY1	955.0NA	540.0NA	355.0NA	1.490UA	885.0NA	460.0NA
22 IIBY2	935.0NA	585.0NA	360.0NA	1.450UA	895.0NA	450.0NA
23 IIBZ1	5.450UA	5.450UA	5.450UA	5.950UA	6.100UA	6.100UA
24 OSCP	-29.90MA	-23.30MA	-15.55MA	-29.35MA	-23.20MA	-15.10MA
25 OSCM	18.75MA	18.10MA	17.10MA	20.35MA	19.90MA	18.70MA
26 ISCP	3.115MA	3.395MA	3.735MA	3.595MA	3.875MA	4.260MA
27 ISCM	-3.180MA	-3.425MA	-3.700MA	-3.615MA	-3.875MA	-4.230MA
28 -XCMRR	67.29 DB	66.45 DB	65.03 DB	72.14 DB	66.64 DB	65.35 DB
29 +XCMRR	64.64 DB	65.17 DB	64.26 DB	70.47 DB	65.28 DB	64.06 DB
30 -YCMRR	76.84 DB	76.42 DB	73.72 DB	75.22 DB	71.64 DB	73.26 DB
31 +YCMRR	81.19 DB	82.83 DB	82.78 DB XA	128.0 DB	78.50 DB	90.14 DB
32 OUTVSP	10.95 V	11.20 V	11.45 V	10.65 V	10.95 V	11.20 V
33 OUTVSM	-11.45 V	-11.35 V	-11.10 V	-10.70 V	-10.40 V	-10.46 V
34 PSRR,15-13	14.13MV/V	-14.89MV/V	-25.95MV/V	21.83MV/V	-14.35MV/V	-34.13MV/V
35 PSRR,18-15	-19.19MV/V	-21.53MV/V	-25.00MV/V	-22.40MV/V	-25.26MV/V	-27.53MV/V
36 XOFF	41.43MV	4.625MV	-23.22MV	-9.900MV	-22.07MV	[illegible]
37 YOFF	-9.275MV	6.275MV	-34.65MV	15.30MV	-12.30MV	-47.70MV
38 IIOX	-110.0NA	-15.00NA	10.00NA	** 710.0NA	** 310.0NA	140.0NA
39 IIOY	20.00NA	-5.000NA	-5.000NA	40.00NA	-10.00NA	10.00NA
40 XFTHRU	-23.33MV	-18.52MV	-14.70MV	-22.25MV	-26.43MV	-29.75MV
41 YFTHRU	3.125MV	3.625MV	5.525MV	11.25MV	8.225MV	6.475MV
42 PINL	-30.60MV	-34.38MV	-30.15MV	-35.17MV	-39.47MV	-44.82MV
43 NINL	-2.100MV	-6.000MV	-6.125MV	-6.075MV	-11.40MV	-14.25MV

* * * * * RADC REFERENCE CODE: 0532RL.ARY:OFF
* * SOURCE TEST SPECIFICATIONS.
* * * * GENERIC TYPE/COMMENTS:

PARM () DEVICE>	1182	1182	1182	1183	1183	1183
NUMB () TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
() FILE>	0	0	0	0	0	0
1 MAXY1(-,-)	10.05 V	10.02 V	10.07 V	9.970 V	10.02 V	10.14 V
2 MAXY1(0,-)	37.00MV	24.60MV	30.35MV	11.40MV	-2.400MV	-6.850MV
3 MAXY1(+,-)	-10.00 V	-10.01 V	-10.08 V	-9.880 V	-9.965 V	-10.10 V
4 MAXY1(-,0)	21.25MV	-10.00MV	-14.45MV	39.50MV	26.65MV	18.35MV
5 OUTOFF	40.80MV	13.60MV	11.20MV	-5.100MV	-16.85MV	-22.00MV
6 MAXY1(+,0)	6.500MV	-16.95MV	-25.85MV	51.85MV	40.90MV	34.85MV
7 MAXY1(-,+)	-10.00 V	-10.07 V	-10.15 V	-9.900 V	-9.990 V	-10.23 V
8 MAXY1(0,+)	53.55MV	12.45MV	-50.00UV	-0.100MV	-15.25MV	-20.50MV
9 MAXY1(+,+)	9.965 V	9.935 V	9.965 V	9.950 V	10.01 V	10.23 V
10 MAXY2(-,-)	9.985 V	9.995 V	9.990 V	9.960 V	10.03 V	10.14 V
11 MAXY2(0,-)	46.35MV	3.150MV	-9.800MV	-15.10MV	-23.55MV	-29.90MV
12 MAXY2(+,-)	-9.990 V	-10.05 V	-10.12 V	-9.805 V	-9.970 V	-10.21 V
13 MAXY2(-,0)	-5.200MV	-29.20MV	-36.60MV	41.35MV	30.35MV	23.35MV
14 OUTOFF	40.45MV	13.00MV	12.70MV	-4.750MV	-15.25MV	-21.40MV
15 MAXY2(+,0)	40.05MV	9.900MV	10.50MV	58.25MV	47.55MV	40.35MV

Table 4. (cont.)

16	MAXY2(-,+)	-10.02 V	-10.05 V	-10.12 V	-9.905 V	-10.00 V	-10.14 V
17	MAXY2(0,+)	25.95MV	8.800MV	20.35MV	-700.0UV	-15.50MV	-22.40MV
18	MAXY2(+,+)	10.01 V	9.995 V	10.05 V	9.950 V	10.00 V	10.12 V
19	IIBX1	830.0NA	530.0NA	350.0NA	1.205UA	845.0NA	530.0NA
20	IIBX2	495.0NA	535.0NA	345.0NA	1.175UA	830.0NA	505.0NA
21	IIBY1	485.0NA	535.0NA	345.0NA	1.185UA	835.0NA	510.0NA
22	IIBY2	835.0NA	495.0NA	340.0NA	1.200UA	835.0NA	515.0NA
23	IIBZ1	5.900UA	5.950UA	5.900UA	-9.200UA	-6.450UA	-6.750UA
24	OSCP	*H -30.10MA	-23.65MA	-15.35MA	*8 -30.35MA	-23.55MA	-15.10MA
25	OSCM	21.15MA	20.50MA	19.25MA	22.80MA	21.70MA	20.25MA
26	ISCP	3.290MA	3.545MA	4.075MA	3.690MA	3.960MA	4.240MA
27	ISCM	-3.320MA	-3.590MA	-4.085MA	-3.640MA	-3.950MA	-4.230MA
28	-XCMRR	67.25 DB	66.77 DB	66.49 DB	68.48 DB	67.19 DB	66.23 DB
29	+XCMRR	65.05 DB	65.36 DB	64.91 DB	66.57 DB	65.45 DB	64.53 DB
30	-YCMRR	74.19 DB	75.87 DB	72.75 DB	72.62 DB	71.50 DB	72.20 DB
31	+YCMRR	95.11 DB	86.04 DB	86.73 DB	85.35 DB	92.15 DB	87.87 DB
32	OUTVSP	11.25 V	11.30 V	11.40 V	11.40 V	11.55 V	11.60 V
33	OUTVSM	-11.55 V	-10.85 V	-11.30 V	-11.50 V	-11.40 V	-11.05 V
34	PSRR,15-13	21.75MV/V	-433.4UV/V	-7.853MV/V	25.90MV/V	4.673MV/V	-4.107MV/V
35	PSRR,18-15	-5.947MV/V	-6.973MV/V	-6.520MV/V	-1.227MV/V	-3.120MV/V	-5.913MV/V
36	XOFF	-32.53MV	-19.68MV	-26.40MV	-4.650MV	9.625MV	15.18MV
37	YOFF	-48.18MV	-17.08MV	-16.90MV	11.20MV	23.18MV	30.25MV
38	IIOX	-65.00NA	-5.000NA	5.000NA	30.00NA	15.00NA	25.00NA
39	IIOY	50.00NA	40.00NA	5.000NA	-15.00NA	0.000 A	-5.000NA
40	XFTHRU	-26.92MV	-27.08MV	-31.35MV	50.77MV	49.82MV	46.60MV
41	YFTHRU	4.475MV	4.925MV	3.950MV	6.750MV	7.225MV	8.325MV
42	PXNL	-36.77MV	-38.73MV	-46.22MV	16.55MV	13.87MV	10.25MV
43	MXNL	-6.800MV	-9.800MV	-10.43MV	16.40MV	16.20MV	12.52MV

= = = = = RADC REFERENCE CODE: 0532RL.ARVZOFF
= = SOURCE TEST SPECIFICATION:
= = = = GENERIC TYPE/COMMENT:

PARM	() DEVICE>	1184	1184	1184	1185	1185	1185
NUMB	() TEMP>	-55 C	25 C	125 C	-55 C	25 C	125 C
	() FILE>	0	0	0	0	0	0
1	MAXY1(-,-)	10.03 V	10.05 V	10.14 V	9.980 V	9.970 V	10.02 V
2	MAXY1(0,-)	29.85MV	14.80MV	23.40MV	19.10MV	9.350MV	10.35MV
3	MAXY1(+,-)	-9.920 V	-9.970 V	-10.06 V	-9.935 V	-9.960 V	-10.02 V
4	MAXY1(-,0)	60.55MV	49.40MV	54.45MV	29.20MV	13.50MV	11.10MV
5	OUTOFF	14.00MV	900.0UV	8.400MV	9.150MV	-5.500MV	-5.200MV
6	MAXY1(+,0)	72.50MV	59.80MV	63.80MV	35.45MV	20.05MV	19.55MV
7	MAXY1(-,+)	-9.920 V	-9.965 V	-10.07 V	-9.935 V	-9.970 V	-10.03 V
8	MAXY1(0,+)	13.40MV	2.700MV	8.250MV	11.50MV	-6.450MV	-6.950MV
9	MAXY1(+,+)	10.03 V	10.05 V	10.13 V	9.965 V	9.955 V	9.995 V
10	MAXY2(-,-)	10.05 V	10.06 V	10.15 V	9.980 V	9.970 V	10.01 V
11	MAXY2(0,-)	6.800MV	-7.050MV	-1.450MV	3.200MV	-14.80MV	-17.20MV
12	MAXY2(+,-)	-9.905 V	-9.945 V	-10.03 V	-9.920 V	-9.955 V	-10.01 V
13	MAXY2(-,0)	62.65MV	40.20MV	51.20MV	24.55MV	9.000MV	8.000MV
14	OUTOFF	14.20MV	1.300MV	9.550MV	9.000MV	-6.500MV	-4.300MV
15	MAXY2(+,0)	79.50MV	70.50MV	78.50MV	47.05MV	33.40MV	35.25MV
16	MAXY2(-,+)	-9.945 V	-10.00 V	-10.09 V	-9.965 V	-9.995 V	-10.06 V
17	MAXY2(0,+)	17.90MV	2.400MV	11.60MV	6.650MV	-8.050MV	-1.800MV
18	MAXY2(+,+)	10.01 V	10.02 V	10.12 V	9.955 V	9.950 V	10.00 V
19	IIBX1	970.0NA	[illegible]	[illegible]	930.0NA	630.0NA	[illegible]
20	IIBX2	[illegible]	620.0NA	395.0NA	910.0NA	600.0NA	[illegible]
21	IIBY1	1.010UA	[illegible]	[illegible]	935.0NA	620.0NA	[illegible]
22	IIBY2	1.020UA	675.0NA	430.0NA	925.0NA	595.0NA	[illegible]
23	IIBZ1	5.550UA	5.500UA	5.450UA	5.850UA	5.200UA	5.800UA

Table 4. (cont)

24 OSCP	-29.00MA	-22.65MA	-14.45MA	-30.00MA	-23.35MA	-15.00MA
25 OSCM	19.40MA	19.15MA	17.95MA	21.70MA	20.60MA	19.15MA
26 ISCP	3.290MA	3.530MA	3.955MA	3.460MA	3.700MA	4.170MA
27 ISCM	-3.300MA	-3.540MA	-3.955MA	-3.485MA	-3.715MA	-4.185MA
28 +XCMRR	67.99 DB	66.80 DB	65.33 DB	67.76 DB	66.33 DB	64.61 DB
29 -XCMRR	66.19 DB	64.63 DB	64.11 DB	65.98 DB	64.81 DB	63.36 DB
30 +YCMRR	73.04 DB	72.32 DB	73.72 DB	73.00 DB	74.03 DB	73.74 DB
31 -YCMRR	83.61 DB	91.60 DB	83.41 DB	84.34 DB	84.26 DB	81.48 DB
32 OUTVSP	11.35 V	11.40 V	11.45 V	11.30 V	11.45 V	11.45 V
33 OUTVSM	-11.10 V	-11.65 V	-10.95 V	-11.20 V	-11.40 V	-10.40 V
34 PSRR,15-13	24.56MV/V	1.200MV/V	-11.82MV/V	16.39MV/V	-3.287MV/V	-12.73MV/V
35 PSRR,18-15	-12.34MV/V	-12.81MV/V	-13.76MV/V	-12.42MV/V	-13.16MV/V	-14.11MV/V
36 XOFF	-22.03MV	-6.950MV	-15.97MV	-12.95MV	-2.400MV	-3.450MV
37 YOFF	-4.025MV	4.300MV	-4.125MV	-6.025MV	8.775MV	9.425MV
38 IIOX	55.00NA	-5.000NA	5.000NA	20.00NA	30.00NA	20.00NA
39 IIOY	-10.00NA	-40.00NA	0.000 A	10.00NA	25.00NA	5.000NA
40 XFTHRU	52.53MV	53.70MV	50.33MV	23.18MV	22.28MV	20.53MV
41 YFTHRU	7.825MV	7.850MV	7.425MV	6.150MV	6.950MV	6.900MV
42 PXNL	20.60MV	18.65MV	10.46MV	1.750MV	-524.8UV	-6.525MV
43 MXNL	13.42MV	12.60MV	8.300MV	1.700MV	-2.175MV	-5.175MV

Table 4. (cont)

R A D C STANDARD LIMIT SET SUMMARY

LIMSUM PROGRAM SUMMARY LISTING
' PRECEEDING A LIMIT VALUE INDICATES A LIMIT NOT REQUIRED BY SPEC
THIS IS AN EXTENDED LIMIT IMPOSED BY RADC T/E

REFERENCE DISK ARRAY=D532RL.ARY:OFF

SOURCE TEST SPEC=

GENERIC TYPE=

TXN/PARAMETER	MIN @ 25C	MAX @ 25C	DELTA LIMIT	MIN @ -55C	MAX @ -55C	DELTA LIMIT	MIN @ 125C	MAX @ 125C	DELTA LIMIT
1 MAXY1(-,-)	9.900 V	10.10 V	-----	9.600 V	10.40 V	-----	9.600 V	10.40 V	-----
2 MAXY1(0,-)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
3 MAXY1(+,-)	-10.10 V	-9.900 V	-----	-10.40 V	-9.600 V	-----	-10.40 V	-9.600 V	-----
4 MAXY1(-,0)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
5 OUTOFF	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
6 MAXY1(+,0)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
7 MAXY1(-,+)	-10.10 V	-9.900 V	-----	-10.40 V	-9.600 V	-----	-10.40 V	-9.600 V	-----
8 MAXY1(0,+)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
9 MAXY1(+,+)	9.900 V	10.10 V	-----	9.600 V	10.40 V	-----	9.600 V	10.40 V	-----
10 MAXY2(-,-)	9.900 V	10.10 V	-----	9.600 V	10.40 V	-----	9.600 V	10.40 V	-----
11 MAXY2(0,-)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
12 MAXY2(+,-)	-10.10 V	-9.900 V	-----	-10.40 V	-9.600 V	-----	-10.40 V	-9.600 V	-----
13 MAXY2(-,0)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
14 OUTOFF	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
15 MAXY2(+,0)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
16 MAXY2(-,+)	-10.10 V	-9.900 V	-----	-10.40 V	-9.600 V	-----	-10.40 V	-9.600 V	-----
17 MAXY2(0,+)	-100.0MV	100.0MV	-----	-400.0MV	400.0MV	-----	-400.0MV	400.0MV	-----
18 MAXY2(+,+)	9.900 V	10.10 V	-----	9.600 V	10.40 V	-----	9.600 V	10.40 V	-----
19 IIBX1	0.000 A	2.000UA	-----	0.000 A	8.500UA	-----	0.000 A	2.000UA	-----
20 IIBX2	0.000 A	2.000UA	-----	0.000 A	8.500UA	-----	0.000 A	2.000UA	-----
21 IIBY1	0.000 A	2.000UA	-----	0.000 A	8.500UA	-----	0.000 A	2.000UA	-----
22 IIBY2	0.000 A	2.000UA	-----	0.000 A	8.500UA	-----	0.000 A	2.000UA	-----
23 IIBZ1	-15.00UA	15.00UA	-----	-15.00UA	15.00UA	-----	-15.00UA	15.00UA	-----
24 OSCP	-30.00MA	0.000 A	-----	-30.00MA	0.000 A	-----	-30.00MA	0.000 A	-----
25 OSCM	0.000 A	30.00MA	-----	0.000 A	30.00MA	-----	0.000 A	30.00MA	-----
26 ISCP	0.000 A	6.000MA	-----	0.000 A	6.000MA	-----	0.000 A	6.000MA	-----
27 ISCM	-6.000MA	0.000 A	-----	-6.000MA	0.000 A	-----	-6.000MA	0.000 A	-----
28 -XCMRR	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----
29 +XCMRR	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----
30 -YCMRR	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----
31 +YCMRR	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----	50.00 DB	'120.0 DB	-----
32 OUTVSP	10.00 V	'20.00 V	-----	10.00 V	'20.00 V	-----	10.00 V	'20.00 V	-----
33 OUTVSM	-20.00 V	'-10.00 V	-----	-20.00 V	'-10.00 V	-----	-20.00 V	'-10.00 V	-----
34 PSRR,15-13	-150.0MV/V	150.0MV/V	-----	-150.0MV/V	150.0MV/V	-----	-150.0MV/V	150.0MV/V	-----
35 PSRR,18-15	-50.00MV/V	50.00MV/V	-----	-50.00MV/V	50.00MV/V	-----	-50.00MV/V	50.00MV/V	-----
36 XOFF	-50.00MV	50.00MV	-----	-100.0MV	100.0MV	-----	-100.0MV	100.0MV	-----
37 YOFF	-50.00MV	50.00MV	-----	-100.0MV	100.0MV	-----	-100.0MV	100.0MV	-----
38 IIOX	-200.0NA	200.0NA	-----	-400.0NA	400.0NA	-----	-400.0NA	400.0NA	-----
39 IIOY	-200.0NA	200.0NA	-----	-400.0NA	400.0NA	-----	-400.0NA	400.0NA	-----
40 XFTHRU	-100.0MV	100.0MV	-----	-100.0MV	100.0MV	-----	-100.0MV	100.0MV	-----
41 YFTHRU	-80.00MV	80.00MV	-----	-80.00MV	80.00MV	-----	-80.00MV	80.00MV	-----
42 PXNL	-60.00MV	60.00MV	-----	-200.0MV	200.0MV	-----	-200.0MV	200.0MV	-----

Table 4. (cont.)

SECTION III
JFET ANALOG SWITCHES
MIL-M-38510/111

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

3.1 INTRODUCTION

This section of the report pertains to the characterization of JFET Analog Switches. Analog switches are very similar to a standard mechanical switch. They have higher "on" resistances (ohms vs. milliohms) and cannot handle as much current (milliamps vs. amps) as their mechanical counterpart. However, analog switches have a longer switch life, are smaller in size, and are more reliable and faster (10^6 operations/sec vs. 200 operations/sec). Table 3-1 lists the JFET analog switches specified for MIL-M-38510/111.

TABLE 3-1 DEVICE TYPES

Device	Generic	Manufacturer	Description
01	181A	Intersil, Siliconix	Dual, 30 ohm SPST switches
02	182A	Intersil, Siliconix	Dual, 75 ohm SPST switches
03	184A	Intersil, Siliconix	Dual, 30 ohm DPST switches
04	185A	Intersil, Siliconix	Dual, 75 ohm DPST switches
05	187A	Intersil, Siliconix	Single, 30 ohm SPDT switches
06	188A	Intersil, Siliconix	Single, 75 ohm SPDT switches
07	190A	Intersil, Siliconix	Dual, 30 ohm SPDT switches
08	191A	Intersil, Siliconix	Dual, 75 ohm SPDT switches

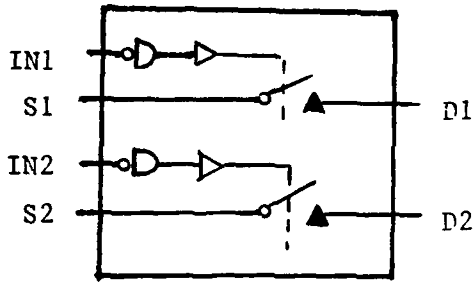
3.2 DESCRIPTION OF DEVICE TYPES

The analog switches listed in Table 3.1 are either two or four N-channel junction-type field effect transistors which operate as switches. The block diagram representations are shown in Figure 3.1. The devices are designed with a turn-off time which is faster than its turn-on time to allow a break-before-make action when switching channels. The switch can be activated by using TTL voltage levels on the logic input of the device. The 75 ohm analog switches can handle a +/- 10 volt signal and the 30 ohm switches can pass a +/- 7.5 volt signal from source to drain.

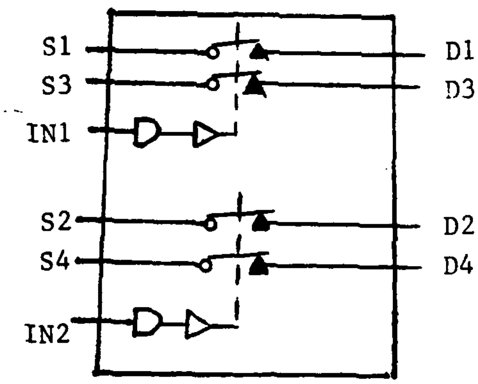
3.3 TEST DEVELOPMENT

The parameters used for characterization of the JFET analog switches are listed in Table 3-2.

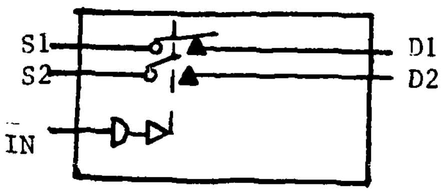
A. Device Type 01 and 02



B. Device Type 03 and 04



C. Device Type 05 and 06



D. Device Type 07 and 08

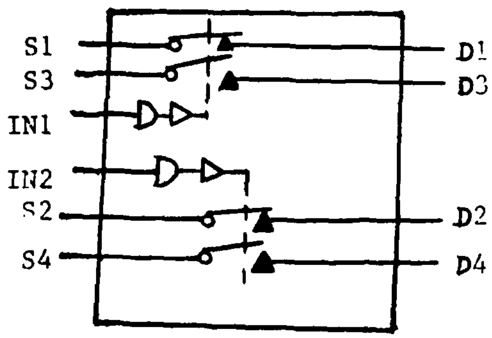


Figure 3-1 Block Diagram

TABLE 3-2 CHARACTERIZATION PARAMETERS

Symbol	Parameter
RDS	Drain to Source (ON) Resistance
$I_{S(OFF)}$	Source leakage current (OFF)
$I_{D(OFF)}$	Drain leakage current (OFF)
$I_D(ON)$, $I_S(ON)$	Channel leakage current
I_{IL}, I_{IH}	Low, High level input current
T_{ON}, T_{OFF}	ON and OFF time
+/- ICC	Positive and negative supply current
I_L	Logic supply current
I_R	Reference supply current
V_{CTE}	charge transfer error
V_{CT}	Cross talk
V_{ISO}	Channel isolation
t_D	Break-before-make time delay

The testing of all dc parameters was performed on a Tektronix 3270, and the ac parameters were tested using bench-top test equipment. The manufacturer's suggested detail specification formed the baseline for the development of the final specification. The original parameter selection was supplemented with additional parameter categories as determined necessary following investigation of specific system applications. The complete final parameter list is representative of manufacturer's inputs, application engineer requirements and specific Air Force system surveys. The list of parameters which were added to the original suggested specification were crosstalk, isolation, charge transfer error and break-before-make time delay. The static test circuit for the above parameters is shown in Figure 3-2.

3.4 TEST RESULTS AND DISCUSSION

Drain to Source ON Resistance (RDS)

The ON resistance is measured by applying the drain voltage and -10mA to the source terminal as specified in the slash sheet. A voltage measurement is performed on the source pin, rather than determining the resistance directly. The limit in the slash sheet is specified as a voltage which correlates to the amount of

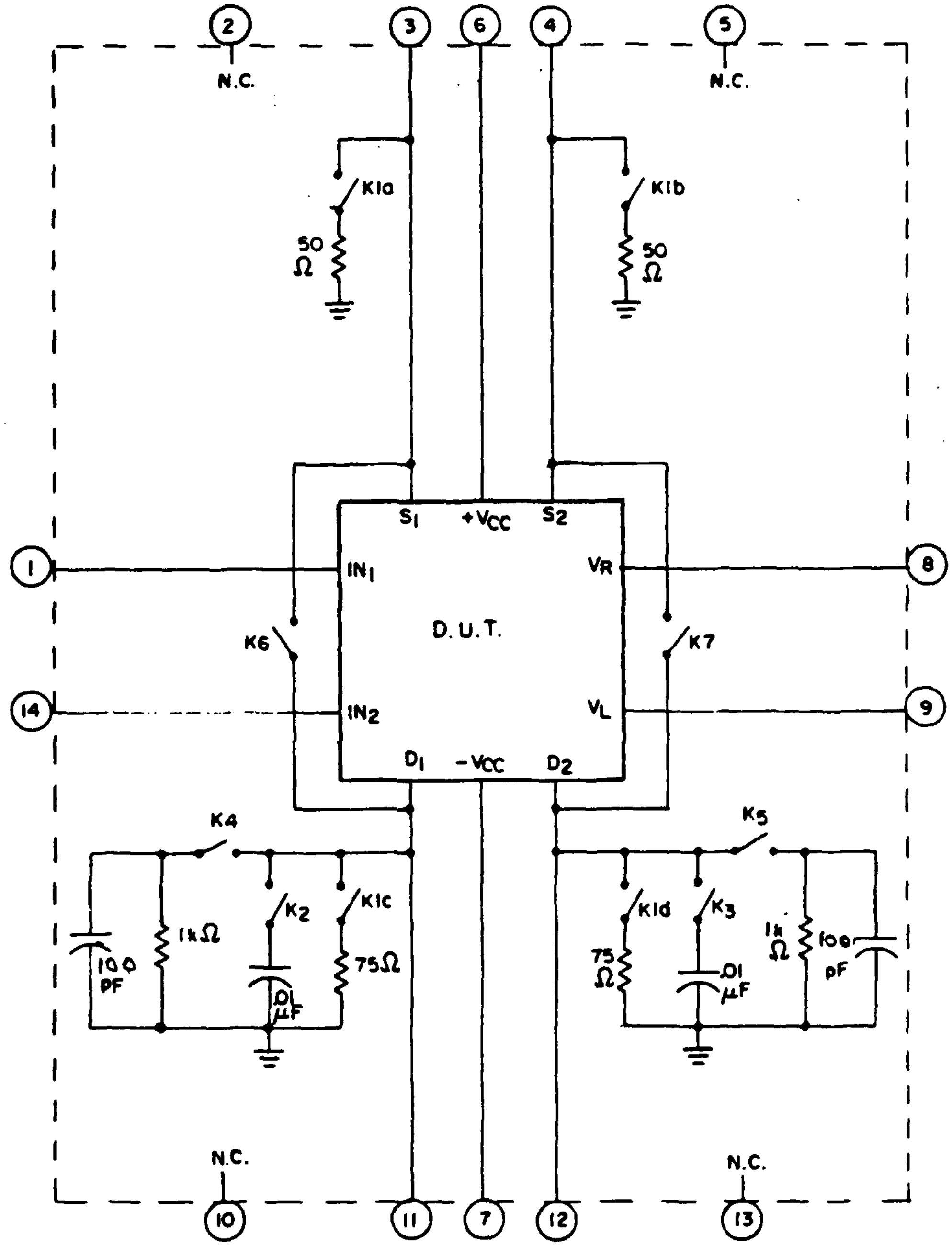


Figure 3-2 Test circuit (static and dynamic tests) for device types 01 and 02.

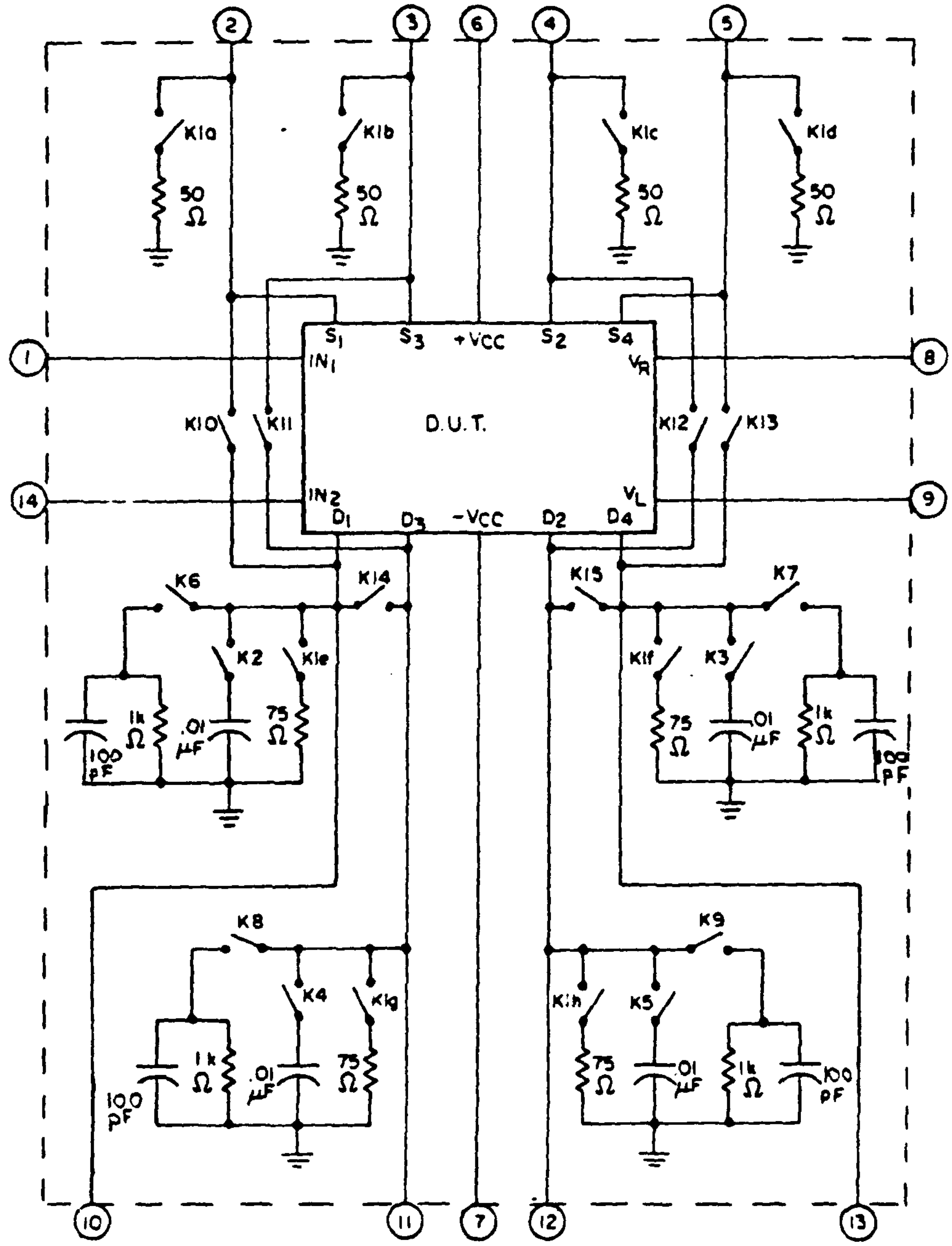


Figure 3-2 Test circuit (static and dynamic tests) for device types 03, 04, 07 and 08.

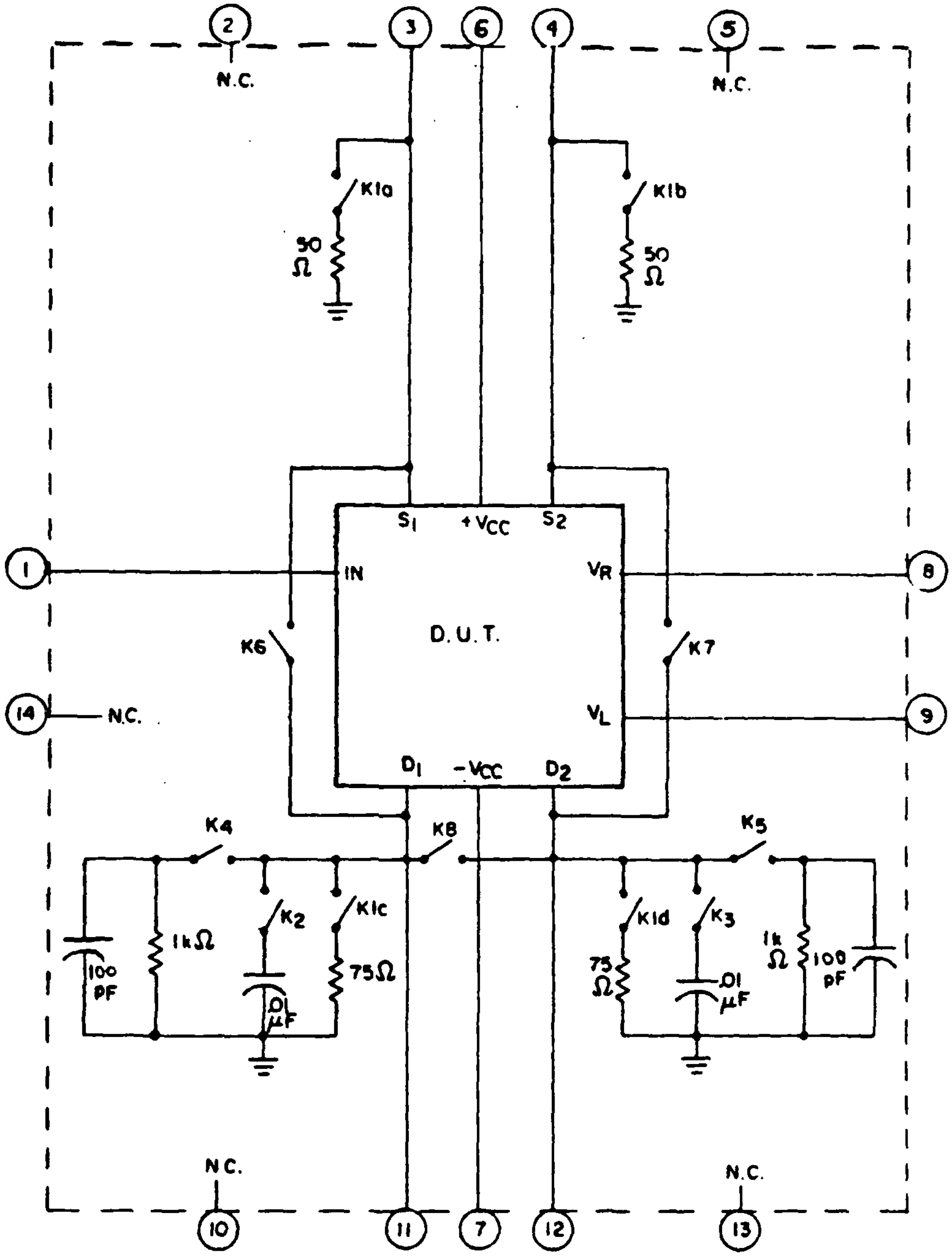


Figure 3-2 Test circuit (static and dynamic tests) for device types 05 and 06.

resistance. An example of this is RDS for device type 01. Drain voltage is -7.5 volts and the limit on the source voltage is -7.8. If the difference between the two voltages is obtained and divided by -10mA, the 30 ohms maximum resistance limit is achieved. An example of a data tabulation and reduction summary recorded from the Tektronix 3270 is shown in Figure 3.3. The figure represents RDS for a test sample of fifteen DG190 devices and reveals a bimodal distribution. This type of distribution is common and can be attributed to different manufacturers or possibly the difference between off-the-shelf vs. vendor samples. All data obtained for RDS was well within the specified limits.

Source (OFF) leakage current (I_S(OFF))

For source leakage current in the OFF state, set the logic input to the specified voltage in order to open the switch under test. Apply the appropriate voltages to the source and drain and measure the current into the source.

Drain OFF leakage current (I_D(OFF))

The Drain (OFF) leakage current is determined in the same manner as I_S(OFF) except the current into the drain is measured.

Channel (ON) leakage current I_D(ON), I_S(ON)

Channel (ON) leakage current is determined by closing the switches and applying a voltage to the source and drain. The drain current I_D(ON) is measured on the first switch and the source current I_S(ON) is measured on all remaining switches.

Input Current (I_{IL}, I_{IH})

The input current is the amount of current associated with each logic input line. Input low current (I_{IL}) is measured by applying ground to the logic pin and measuring the current. A 5 volt input is substituted for ground to measure input high current (I_{IH}).

Supply Current (+/- I_{CC})

The supply current is the amount of current present in the positive and negative supply terminals. The positive and negative supply currents are measured with all logic inputs grounded and repeated with all logic inputs at 5 volts.

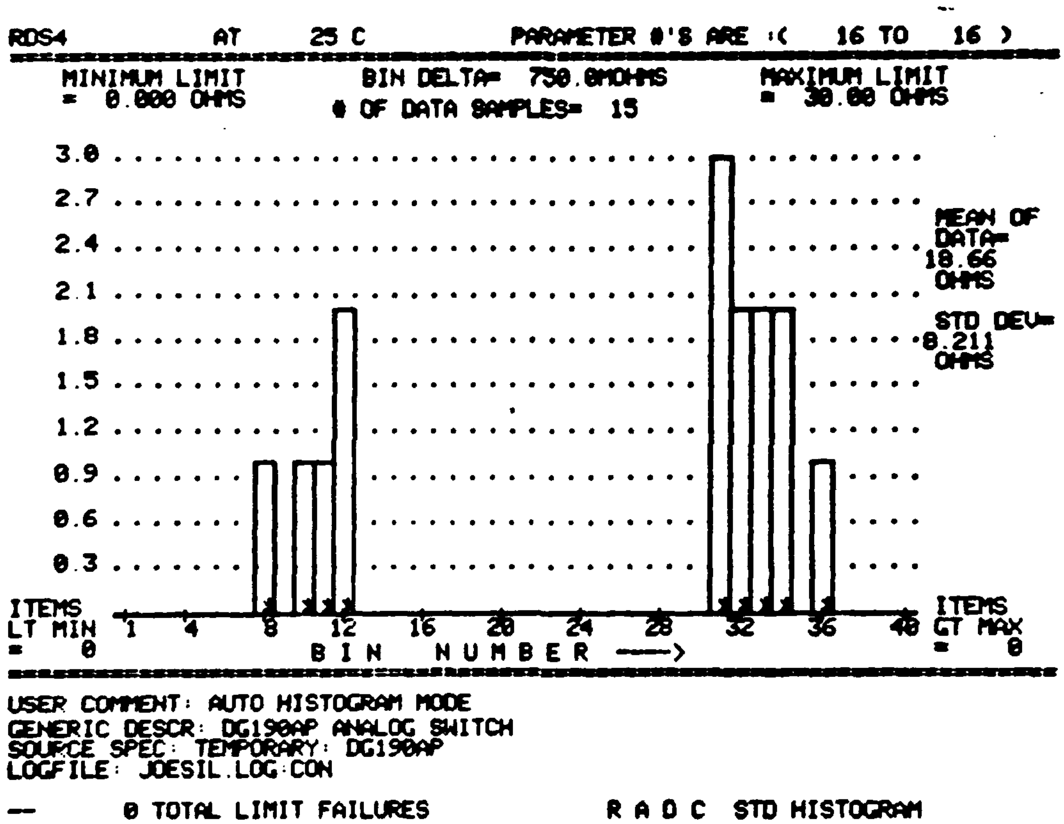


FIG. 3.3

BIMODAL DISTRIBUTION

Logic Supply Current (I_L)

The logic supply current is the amount of current flow into the device's logic supply (V_L) terminal when it is set to 5 volts. The current is first measured with all logic inputs at ground. The second measure is performed with all logic inputs at 5 volts.

Reference Supply Current (I_R)

The amount of current flow out of the reference supply (V_R) terminal of the device is measured for two logic input conditions. The first is with the inputs grounded; the second measurement is performed with the logic inputs at 5 volts. In both cases, the current is measured with the reference supply terminal grounded.

Charge Transfer Error (V_{CTE})

For charge transfer error, the source of the switch is grounded and the logic input pin is clocked with a 3 volt 100KHz 50% duty cycle pulse. A 0.01uf load to ground is placed on the drain and the peak to peak voltage present on the drain terminal is measured.

Cross Talk (V_{CT})

This test is performed only on devices which are monolithic; it does not apply to multi-chip devices. The switches are placed in the closed position. Device type 01, for example, is a dual single pole single throw switch. For this case, a 1 volt peak to peak, 10MHz square wave is placed on source 1, the V_{CT} peak to peak voltage on drain 2 is measured. The reading can either be in mvp-p or dB. The V_{CT} in dB is determined by the following equation:

$$dBV_{CT} = -20 \log (V_{OUT}/V_{IN})$$

This test determines the degree of coupling that exists between two adjacent switches in a multi-switch circuit.

Channel Isolation (V_{ISO})

To perform the channel isolation test, the switch is placed in the open position and a 1Vp-p 10MHz square wave is applied to each source in turn. The magnitude of the signal on the corresponding drain is measured; this indicates the

ability of the open switch to isolate between the source and drain. The limit can be expressed in terms of mVp-p or decibels. The V_{ISO} in db is determined by the following equation:

$$dBV_{ISO} = -20 \log (V_{OUT}/V_{IN})$$

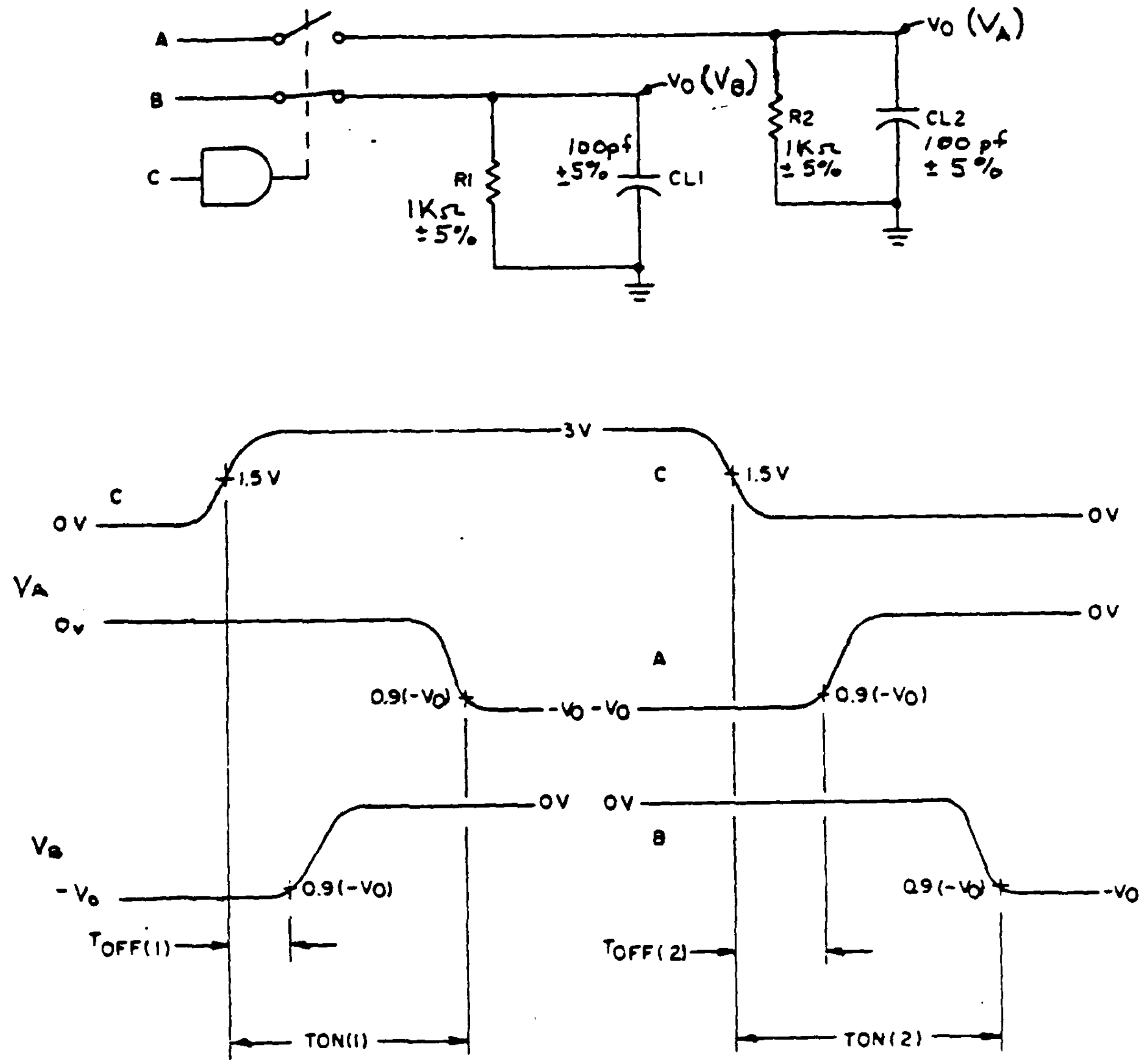
Break-Before-Make Time Delay (t_D)

The break-before-make time delay is only performed on device types 05, 06, 07 and 08. The remaining device types do not have the proper switch configuration for this test. The test circuit and waveforms for the break-before-make test are shown in Figure 3.4. A voltage of -7.5 is applied to the source terminals of device types 05 and 07 (-10V is used for device types 06 and 08). A 3 volt, 1KHz square wave with rise and fall times less than or equal to 10ns is applied to the logic input terminal. A load of 1K ohms in parallel with 100pf is placed on the drain of each switch. As can be seen from the figure, the break-before-make time of switch 1 (t_{D1}) is measured from the 50% point on the rising edge of the logic input pulse to 90% point of the output pulse (V_O is -7.2 volts for device types 05 and 07 and -9.2V for device types 06 and 08). The measurement of t_{D2} is made from the 50% point of the input pulse falling edge to the 90% point of the switch 2 output pulse.

Characterization of the JFET (DG180 series) analog switches has revealed interesting information regarding the relationship between T_{ON} and T_{OFF} of opposite state switches being driven by the same driver within a package (break-before-make action). The manufacturer's guarantee of break-before-make action was found to be false for all cases with testing performed at -55°C (action at 25°C was verified). It was necessary to note this inconsistency in /111 so that users could be made aware of this difference in performance over temperature. The problem arose from the fact that while T_{OFF} basically remained the same across temperature, the T_{ON} was progressively faster as the ambient temperature was lowered (T_{ON} approached T_{OFF}). The break-before-make action is shown in Figure 3.5.

Turn ON and Turn OFF time (T_{ON}, T_{OFF})

The measurement of T_{ON} and T_{OFF} is shown in figure 3.6. The ON and OFF time is a measurement of the amount of time needed to switch the source from 0 to $+V_S$ and from $-V_S$ to 0, respectively.



$T_{D1} = T_{ON(1)} - T_{OFF(1)}$ $T_{D2} = T_{ON(2)} - T_{OFF(2)}$

Figure 3.4 Break-before-make test.

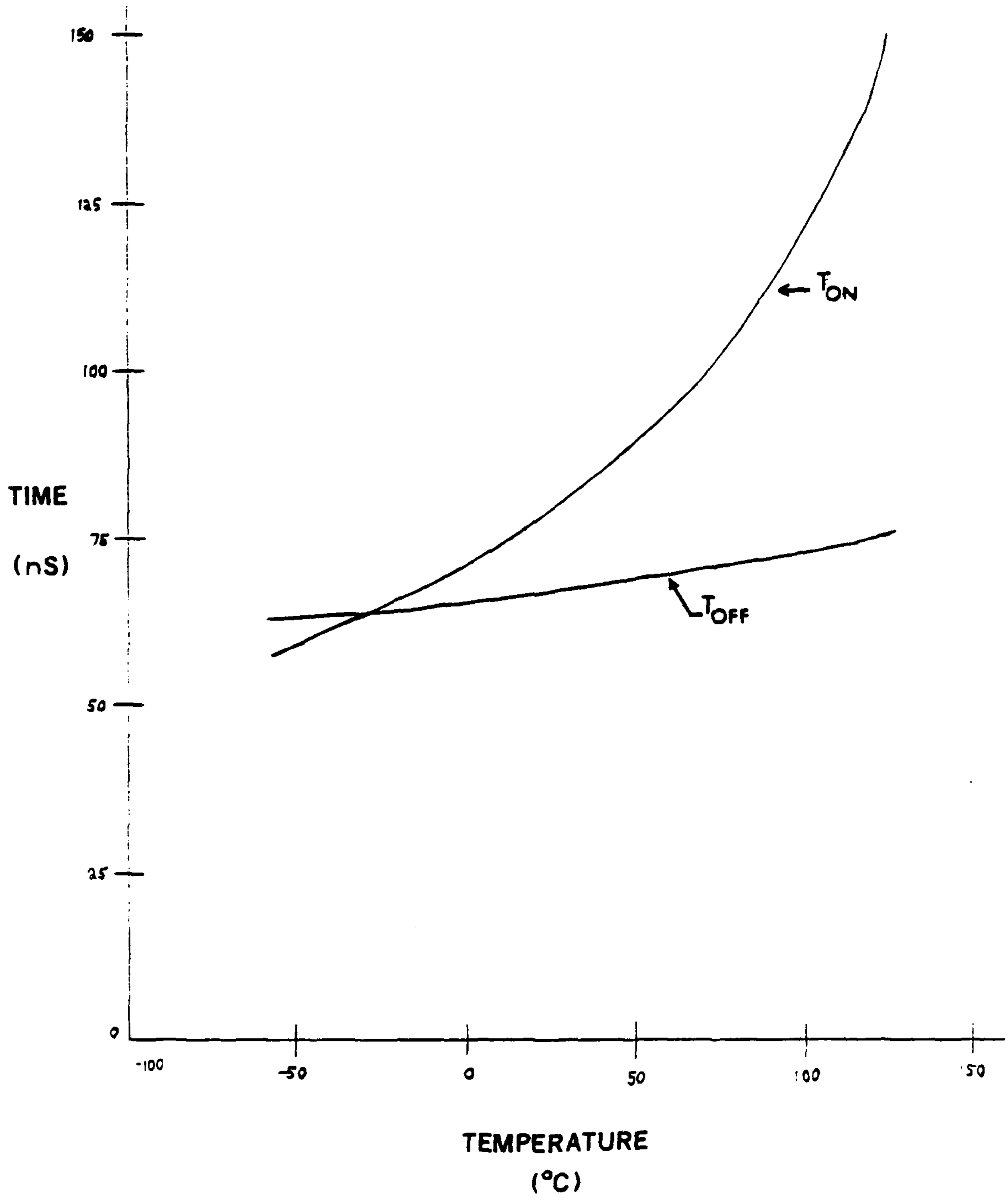
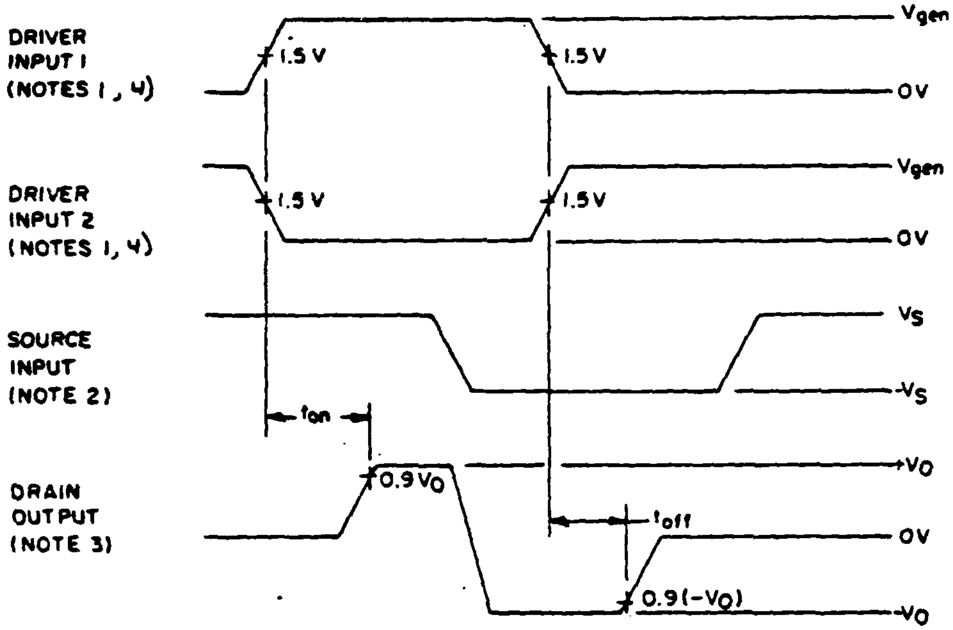


FIG. 3.5
T_{ON} AND T_{OFF} OVER TEMPERATURE



NOTES:

1. The driver pulse generator shall have the following characteristics:

   a. V_{gen} = 0 V to 3.0 V.
   b. Rise time (0.3 V to 2.7v) $\leq$ 10 ns.
   c. Fall time (2.7 V to 0.3 V) $\leq$ 10 ns.

2. The source pulse generator shall have the following characteristics:

   a. V_{gen} = -7.5 V to +7.5 V square wave (device types 01, 03, 05 and 07).
   b. V_{gen} = -10.0 V to +10.0 V square wave (device types 02, 04, 06 and 08).

Figure 3.6 Input-output waveforms for time delay tests.

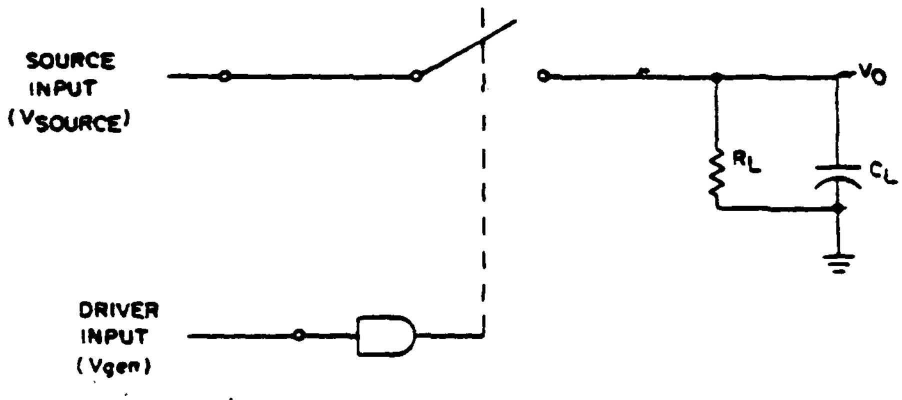
3. For device types 01, 03, 05 and 07:

   a. V_{source} = +7.5 V for T_{on}.
   b. V_{source} = -7.5 V for T_{off}.

For device types 02, 04, 06 and 08:

   a. V_{source} = +10.0 V for T_{on}.
   b. V_{source} = -10.0 V for T_{off}.

4. Driver input 1 shall be used to test all switches for device types 03 and 04, switch 1 for device types 05 and 06 and switches 1 and 2 for device types 07 and 08. Driver input 2 shall be used to test all switches for device types 01 and 02, switch 2 for device types 05 and 06 and switches 3 and 4 for device types 07 and 08.



R_L = 1 kΩ ±5%.
C_L = 100 pf ±5% (C_L includes associated test system capacitance)

Figure 3.6 Input-output waveforms for time delay tests - Continued.

The finalized electrical parameters, conditions and limits for MIL-M-38510/111 are shown in Table 3.3.

An example of Tektronics 3270 test data for device type 07 is shown in Table 3.4. The table reflects the data summary of 15 devices at 25°C.

Special Problem Parameters

Specific parameters fell into the category of special problem parameters since special consideration had to be given in either their measurement technique or limit determination. These parameters along with their respective problem areas are discussed in the subsequent paragraphs.

Switch leakage in the off state is a critical switch parameter since it is representative of dc (or low frequency) isolation performance. The leakage parameters I_S(OFF), I_D(OFF), I_D(ON), and I_S(ON) exhibited special measurement problems at low temperatures. Although switch performance is capable of leakage measurements of 1nA or less at room temperature, condensation (frosting) problems at -55°C result in leakage increases that must be accounted for in assigning parameter limit values at this temperature. Typically, leakage performance increases as ambient temperature drops. This real-world manufacturer testing problem resulted in considerably higher limits being assigned to these leakage parameters than were assigned at room temperature.

The turn-off time parameter (T_{OFF}) was redefined. The manufacturer originally suggested that the turn-off point be specified at the 10% mark on the voltage curve. However, electrical characterization of the switches in question showed that the capacitive load attached to the switch output (drain) caused the 10% value to exist at a point far out on the capacitive "tail" curve. Since this capacitive tail varies with the capacitive load value, the switch is actually open long before this 10% value is achieved. A determination was made on this basis for the 90% point on the output curve to be the point of measurement for T_{OFF}.

Charge transfer error (V_{CTE}) was not originally considered a device manufacturering parameter. However, characterization efforts along with application considerations indicate the importance of this parameter in sample-and-hold as well as other applications. Toggling the input driver causes voltage transitions at the gate of the JFET. These transitions result in output (drain) spikes caused by the gate to drain JFET capacitance C_{gd}. The spiking is a function of the rise time of the transitional voltage at the JFET gate and voltage division of

Characteristic	Symbol	Conditions VL= +5V, VR= GND ±VCC=±15V -55°C <= TA <= 125°C Unless otherwise specified	Device Type	Limits MIN	Limits MAX	Units
Resistance drain-to-source(on)	RDS	VD= -7.5V, IS=-10mA 2/	01,03 05,07		60	Ohms
		VD= -10V, IS= -10mA 2/	02,04 06,08		150	Ohms
Source Leakage current (off)	IS(off)	VD=-10V, VS= 10V +VCC= 10V, -VCC= -20V 2/	ALL	-100	100	nA
		VD= -7.5V, VS= +7.5V 2/	01,03 05,07	-100	100	nA
		VD= -10V, VS= 10V 2/	02,04 06,08	-100	100	nA
Drain leakage current (off)	ID(off)	VD= 10V, VS= -10V +VCC= 10V, -VCC= -20V 2/	ALL	-100	100	nA
		VD= 7.5V, VS= -7.5 V 2/	01,03 05,07	-100	100	nA
		VD= 10V, VS= -10V 2/	02,04 06,08	-100	100	nA
Channel leakage current (on)	ID(on)+ IS(on)	VD= VS= -7.5V 2/	01,03 05,07	-200	200	nA
		VD= VS= -10V 2/	02,04 06,08	-200	200	nA
Low Level input current	IiL	VIN= GND	ALL	-250	-.1	uA
High Level input current	IIH	VIN= 5V	ALL	-2	20	uA
Time to turn on	tON	TA= -55°C, 25°C	01,03 05,07		150	nS
		TA= 125°C			300	nS
Time to turn on	tON	TA= -55°C, 25°C	02,04 06,08		250	nS
		TA= 125°C			350	nS
Time turn off	tOFF	TA= -55°C, 25°C	ALL		130	nS
		TA= 125°C			200	nS
Positive supply current	+ICC	VIN= GND and 5V	01,02 07,08		2.5	mA
			05,06		1.4	mA
		VIN= GND	03,04		5	mA
		VIN= 5V	03,04		1.7	mA
Negative supply current	-ICC	VIN= GND and 5V	01,02 07,08	-8		mA
			05,06	-4.8		mA
		VIN= GND	03,04	-8.8		mA
		VIN= 5V	03,04	-6.4		mA

TABLE 3.3 Electrical Parameter Limits

Characteristic	Symbol	Conditions VL= +5V, VR= GND ±VCC=±15V -55°C <= TA <= 125°C Unless otherwise specified	Device Type	Limits MIN	Limits MAX	Units
Logic supply current	IL	VIN= GND and 5V	01,02,03 04,07,08		7	mA
			05,06		5	mA
Reference supply current	IR	VIN= GND and 5V	ALL	-2.2		mA
Charge transfer error	VCTE	VS= GND TA= 25°C	ALL		20	mV
Crosstalk between channels	VCT 1/	f= 10MHz, Vgen= 1 Vpp TA= 25°C	ALL	60		dB
Single channel isolation	VISO	f= 10MHz, Vgen= 1 Vpp TA= 25°C	ALL	50		dB
Break-before-make time delay	tD	See figure 10	05,06 07,08	5		nS

1/ For monolithic devices only.

2/ The analog switch shall turn "on" with either a low input (VR<= VIL <= 0.8V) or a high input (2V <= VIH <= VL) as follows.

Device Type	VIN	Switch On	Switch Off
01,02	0.8Vdc	1,2	---
	2.0Vdc	---	1,2
03,04	0.8Vdc	---	1,2,3,4
	2.0Vdc	1,2,3,4	---
05,06	0.8Vdc	2	1
	2.0Vdc	1	2
07,08	0.8Vdc	3,4	1,2
	2.0Vdc	1,2	3,4

TABLE 3.3 (cont.) Electrical Parameter Limits

GENERIC DEVICE DESCRIPTION: DG190AP ANALOG SWITCH

RADC REFERENCE CODE: 4444RF ARY CON
TEMPERATURE= 25 C
NUMBER OF DEVICES= 15

PARAMETER	PARM-NUMBS	# LT MIN	MIN SPEC LIMIT	MIN DATA VALUE	MEAN OF DATA	STD DEV	MAX DATA VALUE	MAX SPEC LIMIT	# GT MAX	MIN SER	MAX SER
ICCL	(1 TO 1)	0	0.000 A	555.0UA	878.0UA	210.0UA	1.195MA	1.500MA	0	3	4
ICCH	(2 TO 2)	0	0.000 A	555.0UA	868.3UA	206.4UA	1.175MA	1.500MA	0	3	4
IEEL	(3 TO 3)	0	-5.000MA	-3.860MA	-3.447MA	378.3UA	-2.680MA	0.000 A	0	4	3
IEEH	(4 TO 4)	0	-5.000MA	-3.860MA	-3.446MA	378.8UA	-2.675MA	0.000 A	0	4	3
ILL	(5 TO 5)	0	0.000 A	2.815MA	3.477MA	308.8UA	4.035MA	4.500MA	0	9	6
ILH	(6 TO 6)	0	0.000 A	2.815MA	3.476MA	308.3UA	4.030MA	4.500MA	0	9	6
IRL	(7 TO 7)	0	-2.000MA	-1.095MA	-930.3UA	93.15UA	-760.0UA	0.000 A	0	3	9
IRH	(8 TO 8)	0	-2.000MA	-1.095MA	-930.0UA	92.72UA	-760.0UA	0.000 A	0	3	9
IINL1	(9 TO 9)	0	-250.0UA	-60.75UA	-47.04UA	8.375UA	-34.85UA	0.000 A	0	58	9
IINL2	(10 TO 10)	0	-250.0UA	-56.70UA	-45.63UA	7.941UA	-32.40UA	0.000 A	0	2	9
IINH1	(11 TO 11)	0	0.000 A	0.000 A	0.000 A	0.000 A	0.000 A	10.00NA	0	1	2
IINH2	(12 TO 12)	0	0.000 A	0.000 A	0.000 A	0.000 A	0.000 A	10.00NA	0	1	2
RDS1	(13 TO 13)	0	0.000 OHMS	5.645 OHMS	18.76 OHMS	8.617 OHMS	26.25 OHMS	30.00 OHMS	0	59	8
RDS2	(14 TO 14)	0	0.000 OHMS	5.615 OHMS	18.53 OHMS	8.436 OHMS	26.45 OHMS	30.00 OHMS	0	59	8
RDS3	(15 TO 15)	0	0.000 OHMS	5.725 OHMS	18.53 OHMS	8.274 OHMS	25.35 OHMS	30.00 OHMS	0	59	9
RDS4	(16 TO 16)	0	0.000 OHMS	5.815 OHMS	18.66 OHMS	8.211 OHMS	26.35 OHMS	30.00 OHMS	0	59	10
ID(OFF)1	(17 TO 17)	0	0.000 A	0.000 A	33.33PA	21.60PA	60.00PA	1.000NA	0	2	57
ID(OFF)2	(18 TO 18)	0	0.000 A	30.00PA	44.00PA	10.56PA	60.00PA	1.000NA	0	2	58
ID(OFF)3	(19 TO 19)	0	0.000 A	30.00PA	46.67PA	11.75PA	60.00PA	1.000NA	0	2	56
ID(OFF)4	(20 TO 20)	0	0.000 A	0.000 A	32.00PA	20.07PA	60.00PA	1.000NA	0	2	57
IS(OFF)1	(21 TO 21)	0	0.000 A	50.00PA	89.33PA	34.32PA	150.0PA	1.000NA	0	2	57
IS(OFF)2	(22 TO 22)	0	0.000 A	60.00PA	98.67PA	40.51PA	180.0PA	1.000NA	0	2	59
IS(OFF)3	(23 TO 23)	0	0.000 A	50.00PA	74.67PA	16.42PA	100.0PA	1.000NA	0	2	58
IS(OFF)4	(24 TO 24)	0	0.000 A	60.00PA	78.00PA	11.46PA	100.0PA	1.000NA	0	2	60
ID+IS(ON)1	(25 TO 25)	0	0.000 A	40.00PA	50.00PA	5.345PA	60.00PA	2.000NA	0	6	5
ID+IS(ON)2	(26 TO 26)	0	0.000 A	0.000 A	10.00PA	14.64PA	30.00PA	2.000NA	0	1	2
ID+IS(ON)3	(27 TO 27)	0	0.000 A	0.000 A	4.000PA	10.56PA	30.00PA	2.000NA	0	1	10
ID+IS(ON)4	(28 TO 28)	0	0.000 A	0.000 A	0.000 A	0.000 A	0.000 A	2.000NA	0	1	2
TON11	(29 TO 29)	0	0.000 S	68.50NS	86.85NS	26.03NS	183.5NS	150.0NS	2	5	56
TOFF11	(30 TO 30)	0	0.000 S	52.00NS	57.03NS	4.160NS	65.00NS	130.0NS	0	8	58
TOFF13	(31 TO 31)	0	0.000 S	51.00NS	56.87NS	5.097NS	71.00NS	130.0NS	0	6	60
TON13	(32 TO 32)	0	0.000 S	77.00NS	90.37NS	17.71NS	174.5NS	150.0NS	3	3	56
TON22	(33 TO 33)	0	0.000 S	72.50NS	88.04NS	21.76NS	174.0NS	150.0NS	2	6	56
TOFF22	(34 TO 34)	0	0.000 S	52.00NS	57.30NS	3.583NS	64.50NS	130.0NS	0	8	59
TOFF24	(35 TO 35)	0	0.000 S	53.00NS	57.17NS	3.203NS	64.50NS	130.0NS	0	7	59
TON24	(36 TO 36)	0	0.000 S	71.50NS	83.92NS	19.27NS	171.5NS	150.0NS	3	5	58

Table 3.4 Data Tabulation Summary

C_{gd} and C_{load}. The equation representing this action is as follows:

$$V_{Spike\ Drain} = V_{JFET\ gate} \times \frac{C_{gd}}{C_{load}}$$

Measurements of this parameter have shown that no significant difference in spike amplitude for a given driver-JFET switch combination exists across the military temperature range. The decision was made to evaluate this parameter at 25°C with the frequency of test to be at initial qualification and at six month intervals.

Single channel isolation (V_{ISO}) and crosstalk between channels (V_{CT}) were not suggested by manufacturers to be included in the final detail specification. Discussion with users at JC-41 meetings and elsewhere found these parameters to be of importance. V_{ISO} measures the effectiveness of a single switch in an open state in preventing high frequency ac signals from passing from source to drain.

Investigation has verified that an input to output isolation of 60db at 10MHz is essential and achievable for the DG180 family. A test frequency of 10MHz was selected for the isolation test since many users select DG180 switches for use in this range.

Finally, the break-before-make parameter was added to the detail specification. For switches in opposite states driven by a common driver, break-before-make action is necessary in applications where the sources of two switches cannot be shorted together. Characterization efforts have shown (as previously discussed) that break-before-make action may not occur at -55°C due to a constant turn-off speed over temperature coupled with the decreasing turn-on speed as it approaches -55°C. Appropriate notes were added to the final detail specification to warn the user of this unexpected action for a component commercially advertised as having break-before-make capability.

Limit Determination

Upon completion of the final parameter selection list, determination of the electrical limits for the selected parameters was performed. Detailed electrical characterization procedures are required for meaningful values to be obtained.

The concerns for all parameter limits are the same: (1) selection of limits which are specific and accurately represent the component capability, and (2) selection of limits which will be tolerable for the manufacturer during device testing before shipment. The intent of JC-41 committee meetings is to allow adequate technical exchange to balance the concerns of government and industry. The general category of parameter limit assignment is affected by the specific parameter in question, along with electrical characterization findings. The capability of a parameter to function across the military temperature range, as well as the need to perform wide temperature range measurement, is considered in the determination of applicable parameter limits. The frequency of parameter limit testing (100%, lot sample, etc.) is determined after limit selection, and is based on process variations that might surface as part-to-part or lot-to-lot inconsistencies.

The general breakdown of parameter temperature testing and frequency of testing (defined above) is represented as follows:

(1) All dc electrical parameters are measured across the temperature range on a 100% basis. These include R_{DS} ("on" resistance), all leakages ($I_{D(OFF)}$, $I_{S(OFF)}$, etc.), logic input current (I_{IL} and I_{IH}), and power supply currents.

(2) All ac parameters are measured at 25°C. The following parameters are tested at initial qualification and at six month periodic inspection intervals: V_{CTE} (charge transfer error), V_{CT} (crosstalk), V_{ISO} (isolation), and T_D (break-before-make). These parameters The T_{ON} and T_{OFF} ac parameters are measured 100% at 25°C and lot sample tested at -55°C and 125°C. Refer to MIL-M-38510/111 (Table 2-Page 7 and Table 3-Page 29) and MIL-STD-883C for numerical subgroup assignments and definitions of the respective subgroup categories.

Characterization Findings

The parameter and limit selections for the DG180 JFET analog switch family have been determined after an exhaustive in-house characterization effort which considered other parameters in addition to those finally selected. Such areas

included bandpass capability of a closed switch (f+), "ON" resistance variation as a function of analog signal voltage, and "ON" resistance matching tolerance of switches within a given package. These parameters have been rejected either because of their questionable interest to the general population of application engineers, or because they are not critical to device performance or reliability.

In addition to parameter selection and limit determination, the electrical characterization effort included determination of burn-in techniques as appropriate to the total DG180 JFET switch family. Much effort was spent in the determination of these techniques since the DG180 JFET switch family represents the most complex combination of technology requirements and fabrication procedures. Technology involvement includes Standard Bipolar, Schottky, and MOS technologies appear on a single chip. This is further complicated by the fact that this chip drives a JFET device. Considering the fact that this microcircuit is a multi-chip device (driver chips with JFET chips), extreme care must be given to the selection of appropriate burn-in screening techniques to insure reliability for military applications. The selected burn-in configurations were generated from manufacturer input and from results obtained from burn-in test configurations and fixtures developed in-house.

3.5 CONCLUSION AND RECOMMENDATIONS

The analog switches from the various vendors fully meet the requirements of MIL-M-38510/111 when tested.

3.6 BIBLIOGRAPHY

Intersil Catalog, "Hot Ideas in CMOS" (1983/84).

SECTION IV

CMOS Analog Switches

MIL-M-38510/105, /116 and /123

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

4.1 INTRODUCTION

This section of the report pertains to the characterization of CMOS analog switches. The switches possess many benefits, among them are fast switching speeds and very low power dissipation. Table 4.1 list the analog switches specified for MIL-M-38510 /105 /116 and /123. The device types covered by these slash sheets are all TTL input compatible unless denoted otherwise.

TABLE 4.1 DEVICE TYPES SPECIFIED

/ 105 MICROCIRCUIT LINEAR CMOS HIGH LEVEL ANALOG SWITCH WITH DRIVER

DEVICE	GENERIC	MANUFACTURER	DESCRIPTION
01	5040	H,I,S	One-Channel, 75 ohm, SPST Switch
02	5041	H,I,S	Two-Channel, 75 ohm, SPST Switch
03	5042	H,I,S	One-Channel, 75 ohm, SPDT Switch
04	5043	H,I,S	Two-Channel, 75 ohm SPDT Switch
05	5044	H,I,S	One-Channel, 75 ohm DPST Switch
06	5045	H,I,S	Two-Channel, 75 ohm DPST Switch
07	5046	H,I,S	One-Channel, 75 ohm DPDT Switch
08	5047	H,I	One-Channel, 75 ohm DPST Switch

/ 116 MICROCIRCUIT,LINEAR,CMOS ANALOG SWITCH WITH DRIVER

DEVICE	GENERIC	MANUFACTURER	DESCRIPTION
01	300	H,I,S	Two-channel, SPST,TTL Input Compatible
02	301	H,I,S	One-channel, SPDT,TTL Input Compatible
03	302	H,I,S	Two-channel, DPST,TTL Input Compatible

04	303	H,I,S	Two-channel, SPDT,TTL Input Compatible
05	304	H,S	Two-channel,SPDT,CMOS Input Compatible
06	305	H,S	One-channel,SPDT,CMOS Input Compatible
07	306	H,S	Two-channel,DPST,CMOS Input Compatible
08	307	H,S	Two-channel,SPDT,CMOS Input Compatible

/123 MICROCIRCUIT, LINEAR CMOS, NEGATIVE LOGIC ANALOG SWITCH

DEVICE	GENERIC	MANUFACTURER	DESCRIPTION
01	300	H,I,S	Dual SPST Switch
02	301	H,I,S	Quad SPST Switch

* MANUFACTURER CODE : H-HARRIS I-INTENSIL S-SILICONIX

4.2 DESCRIPTION OF DEVICE TYPES

One of the improvements that CMOS analog switches have over JFET switches is that latch-up has been eliminated. The CMOS analog switches covered under MIL-M-38150 /105 possess an analog input signal range of +/-15 volts, very low input and output leakage currents, and high current capability . The devices covered by /116 have low "on" resistance and a fast switching time. Finally, the /123 family devices are low power and have negative logic input. The terminal connections for the device types covered by the three specifications are shown in figure 4.1.

4.3 TEST DEVELOPMENT

The manufacturers' suggested detail specification were used as the baseline document for the development of the final generated military specifications: Additional parameters determined necessary through RADC

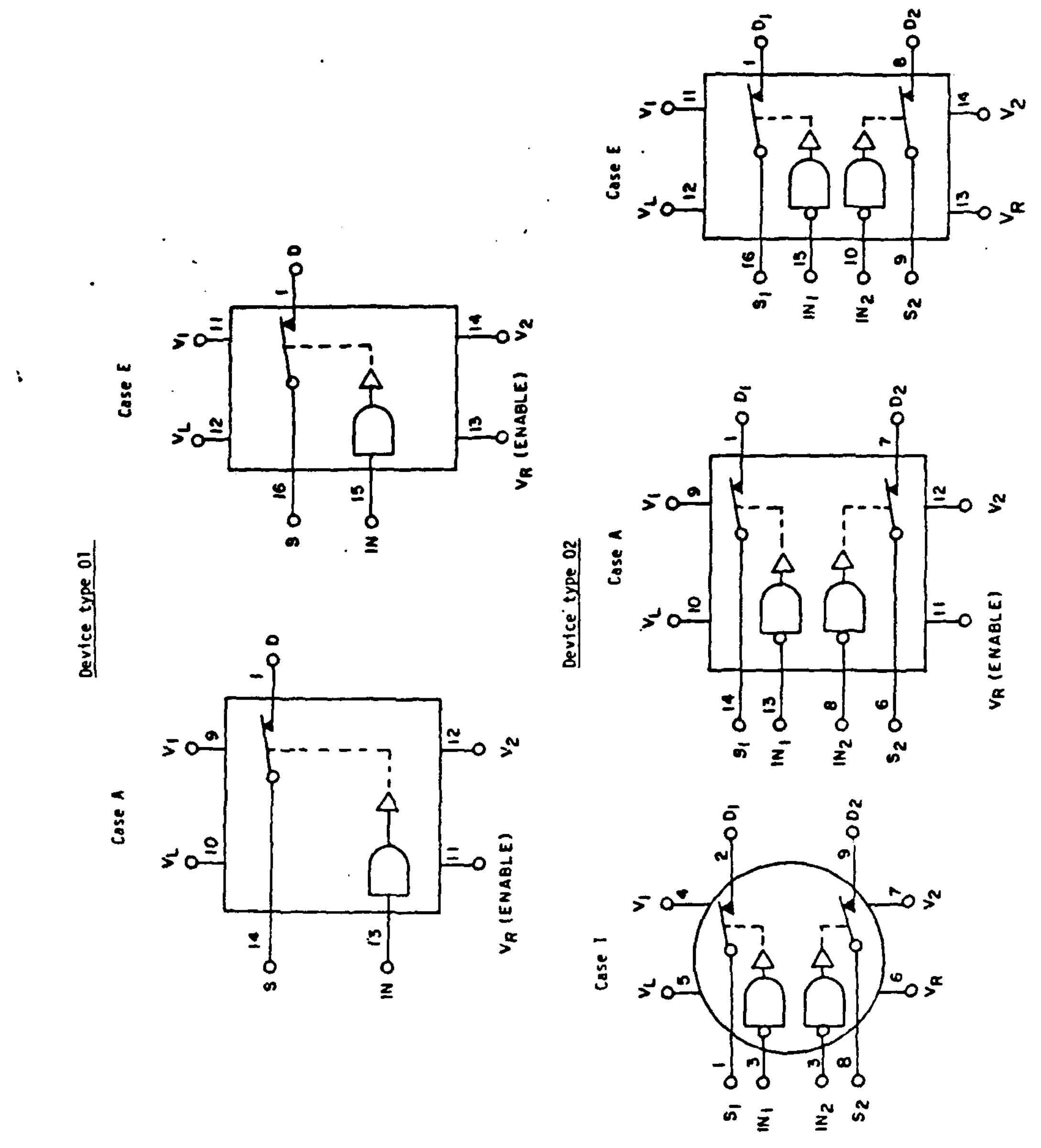


Figure 4.1 Terminal Connection /105

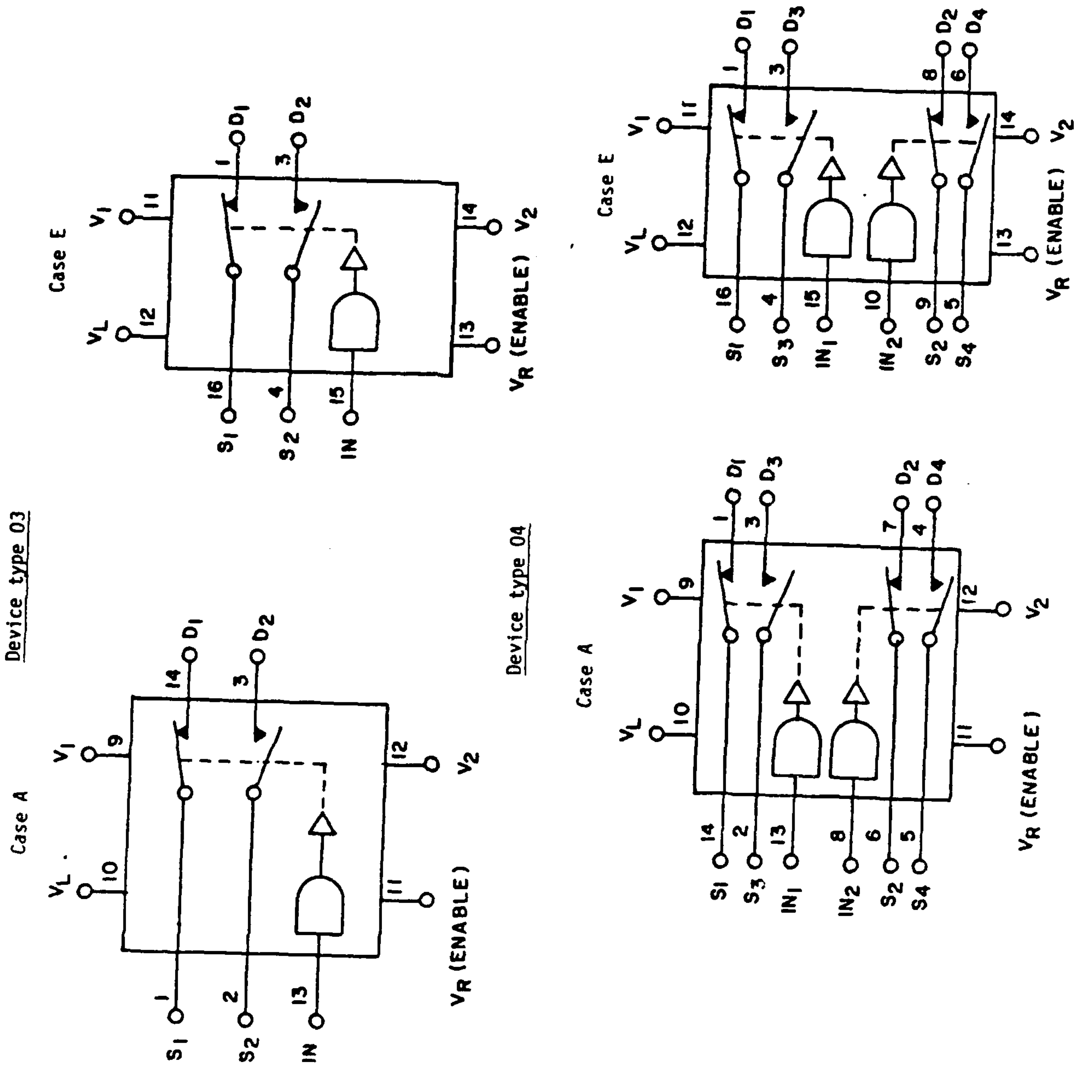
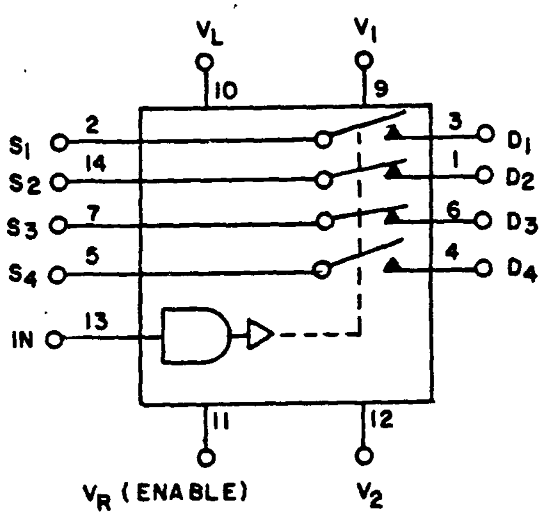


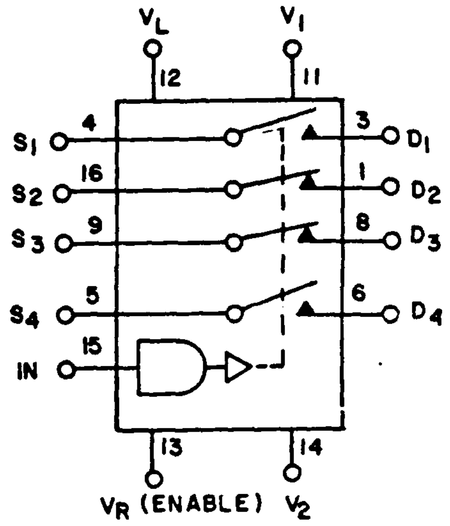
Figure 4.1 cont. Terminal Connections /105

Device type 07

Case A

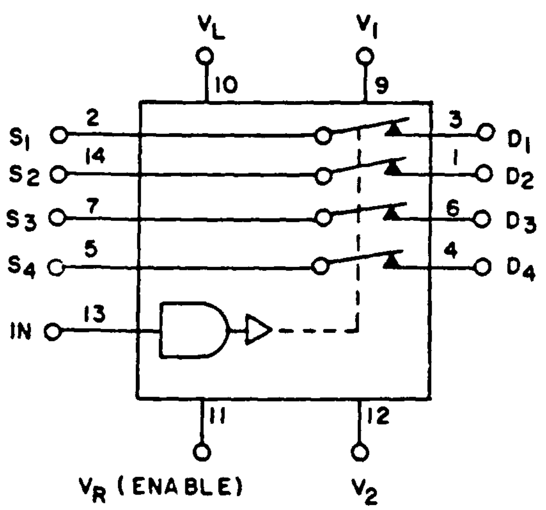


Case E



Device type 08

Case A



Case E

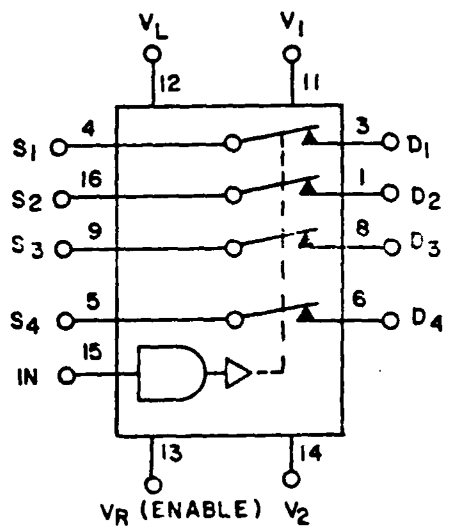


Figure 4.1 cont. Terminal Connection /105

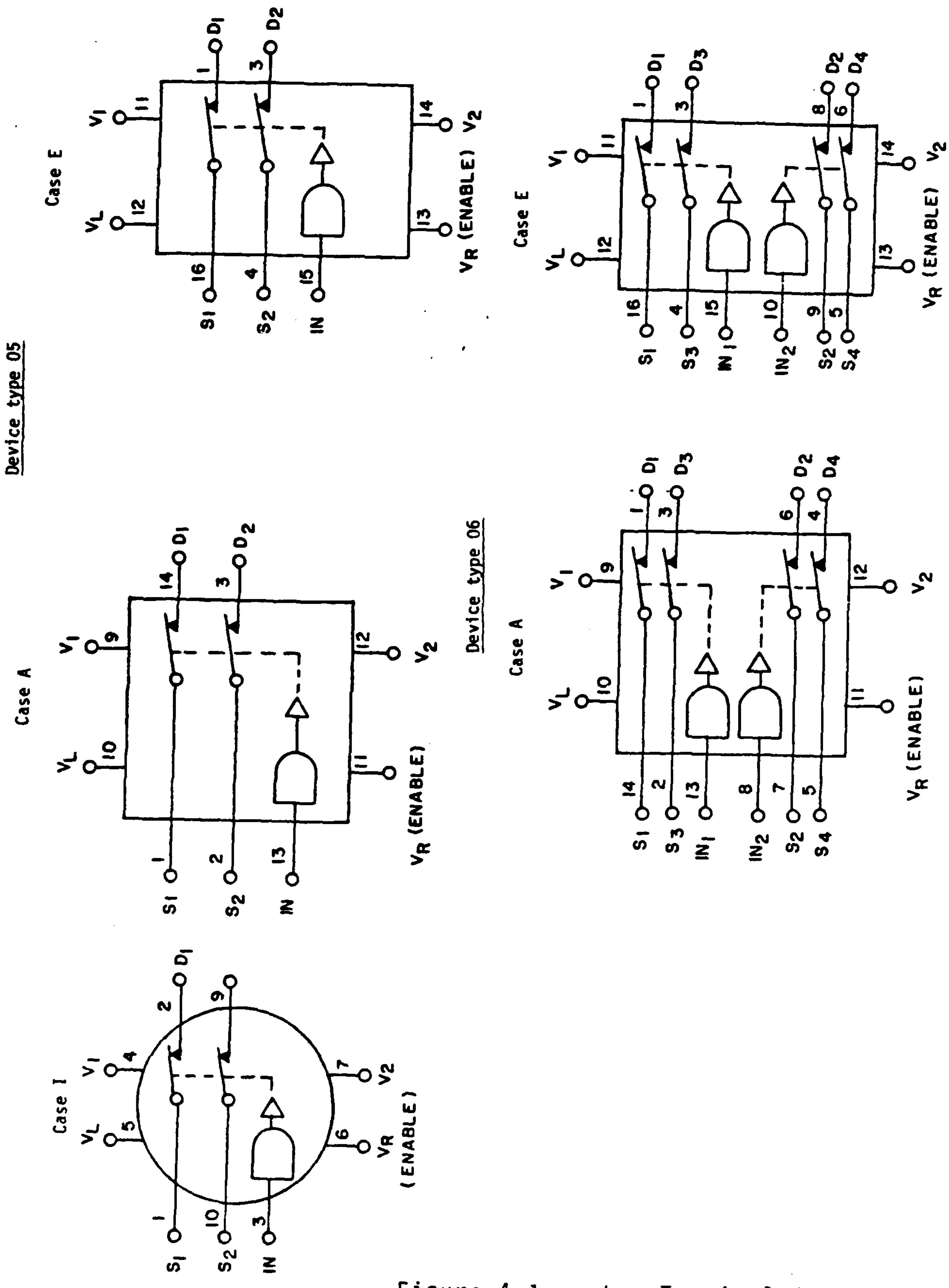
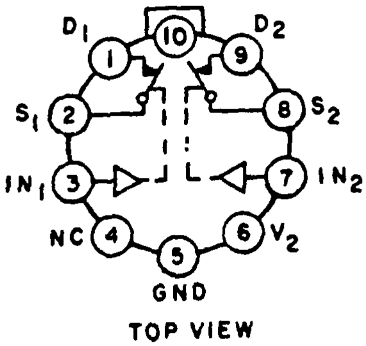


Figure 4.1 cont. Terminal Connection
/105

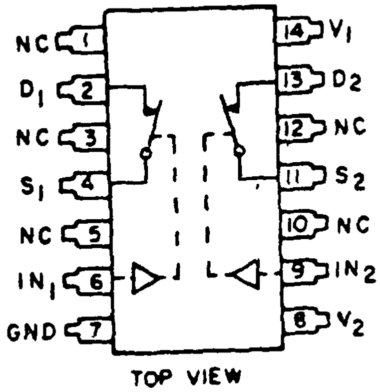
Device types 01 and 05

Case I

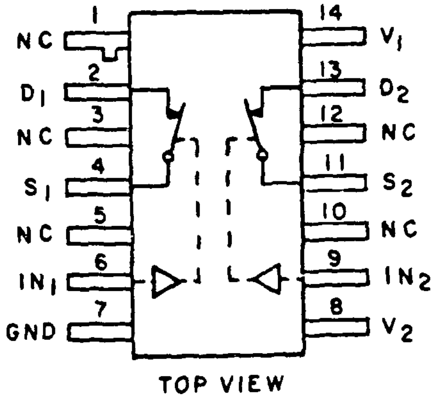
V_1 (SUBSTRATE AND CASE)



Case C



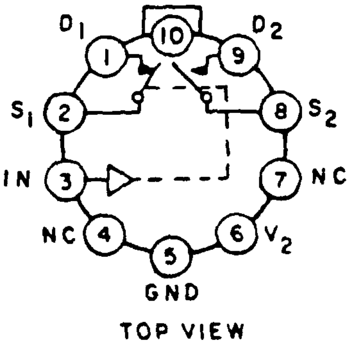
Case D



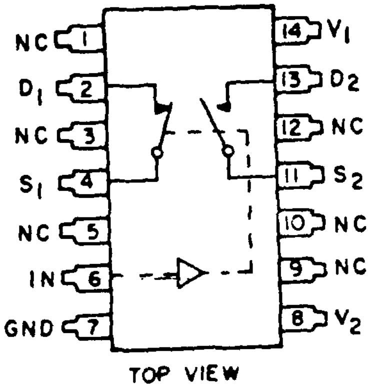
Device types 02 and 06

Case I

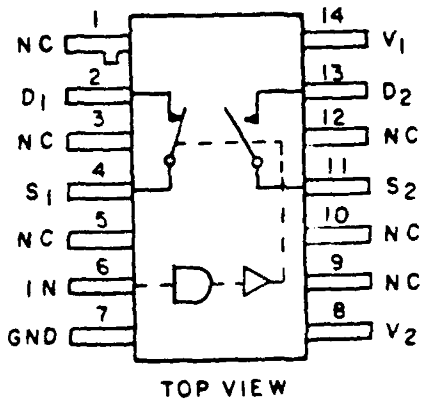
V_1 (SUBSTRATE AND CASE)



Case C



Case D

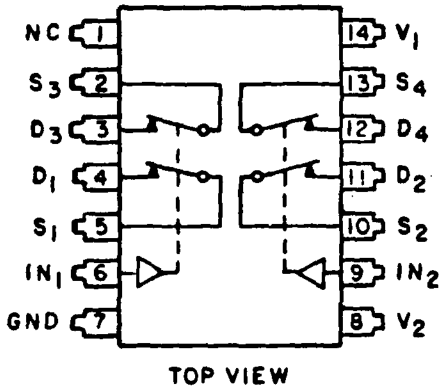


Switch states are for logic "1" input
(Positive logic)

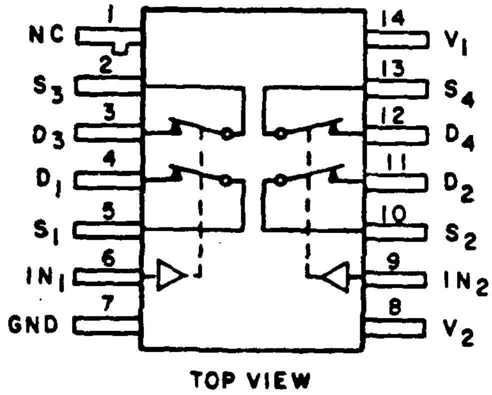
Figure 4.1 cont. Terminal Connection /116

Device types 03 and 07

Case C

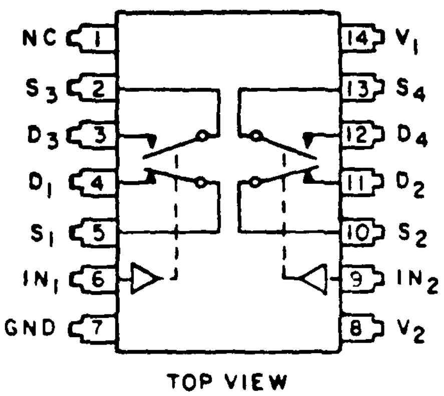


Case D

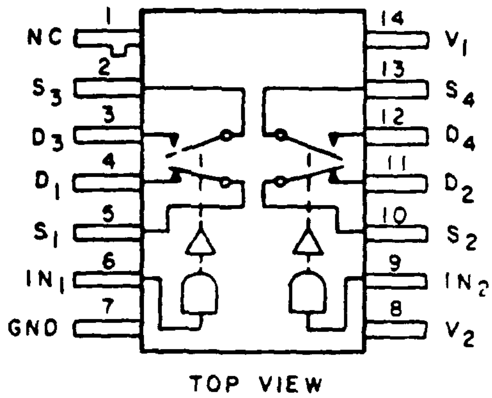


Device types 04 and 08

Case C



Case D

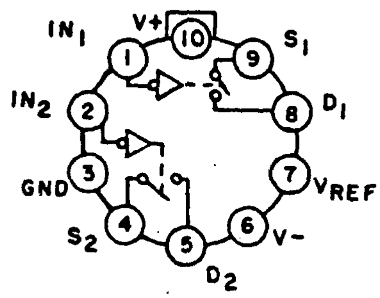


Switch states are for logic "1" input
(Positive logic)

Figure 4.1 cont. Terminal Connection /116

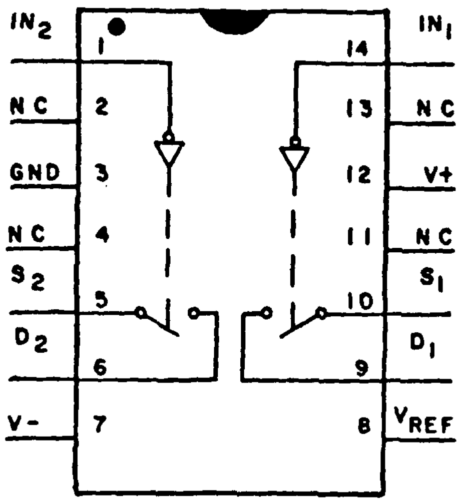
Device type 01

Case 1



Device type 01

Case C



Device type 02

Case E

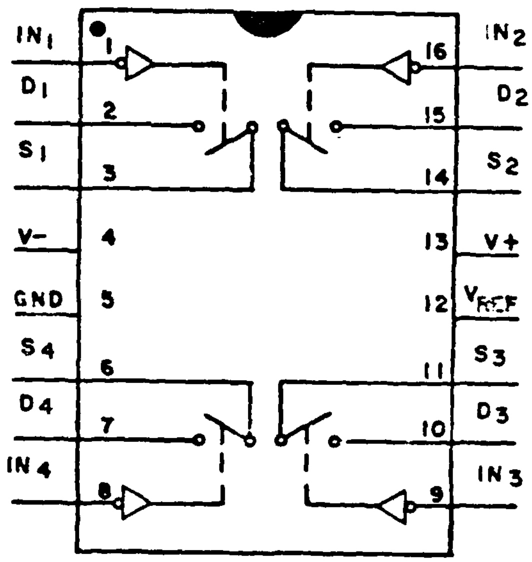


Figure 4.1 cont. Terminal Connection /123

Characteristic	Symbol	Conditions $V_{CC} = \pm 15V$ unless otherwise specified		Temperature	Device type	Limits Min	Limits Max	Units
Drain - Source "ON" resistance	R_{DS}	(See figure 3)	$V_D = -10$ V, $I_S = 10$ mA	$T_C = -55°C, 25°C$	All	---	75	Ω 1/
				$T_C = 125°C$	All	---	150	
			$V_D = 10$ V, $I_S = -10$ mA	$T_C = -55°C, 25°C$	All	---	75	
				$T_C = 125°C$	All	---	150	
		$V_{CC} = \pm 10$ V (See figure 3)	$V_D = -7.5$ V, $I_S = 10$ MA	$T_C = 55°C, 25°C$	All	---	75	
				$T_C = 125°C$	All	---	150	
			$V_D = 7.5$ V, $I_S = -10$ mA	$T_C = -55°C, 25°C$	All	---	75	
				$T_C = 125°C$	All	---	150	
Channel "ON" leakage current	$I_{D(ON)}$	(See figure 4) (See 3.4.1 for V_{IN})	$V_S = V_D = 10$ V	$T_C = -55°C, 125°C$	All	-200	[illegible]	nA
				$T_C = 25°C$	All	-2	[illegible]	
			$V_S = V_D = -10$ V	$T_C = -55°C, 125°C$	All	-200	200	
				$T_C = 25°C$	All	-2	2	
Drain "OFF" leakage current	$I_{D(OFF)}$	(See figure 5) (See 3.4.1 for V_{IN})	$V_S = -10$ V, $V_D = 10$ V	$T_C = -55°C, 125°C$	All	-100	100	
				$T_C = 25°C$	All	-1	1	
			$V_S = 10$ V, $V_D = -10$ V	$T_C = -55°C, 125°C$	All	-100	100	
				$T_C = 25°C$	All	-1	1	
Source "OFF" leakage current	$I_{S(OFF)}$	(See figure 6) (See 3.4.1 for V_{IN})	$V_S = 10$ V, $V_D = -10$ V	$T_C = -55°C, 125°C$	All	-100	100	
				$T_C = 25°C$	All	-1	1	
			$V_S = -10$ V, $V_D = 10$ V	$T_C = -55°C, 125°C$	All	-100	100	
				$T_C = 25°C$	All	-1	1	
Input current, input voltage low	I_{IL}	$V_{IN} = 0$ V	(See figure 7)	$T_C = -55°C, 25°C$	All	-1	0	µA
				$T_C = 125°C$	All	-10	0	
Input current, input voltage high	I_{IH}	$V_{IN} = 2.4$ V, 5 V	(See figure 7)	$T_C = -55°C, 25°C$	All	0	1	
				$T_C = 125°C$	All	0	10	
Positive supply current	$+I_{CC}$	$V_{IN} = 0$ V, 5 V	(See figure 8)	$T_C = -55°C, 25°C$	All	---	10	
				$T_C = 125°C$	All	---	100	
Negative supply current	$-I_{CC}$	$V_{IN} = 0$ V, 5 V	(See figure 8)	$T_C = -55°C, 25°C$	All	-10	---	
				$T_C = 125°C$	All	-100	---	
Logic supply current	$+I_L$	$V_{IN} = 0$ V, 5 V	(See figure 8)	$T_C = -55°C, 25°C$	All	---	10	
				$T_C = 125°C$	All	---	100	
Reference supply current	$-I_R$	$V_{IN} = 0$ V, 5 V	(See figure 8)	$T_C = -55°C, 25°C$	All	-10	---	µA
				$T_C = 125°C$		-100	---	
Turn on time	t_{on}	(See figure 9)		$T_C = -55°C$		---	275	ns
				$T_C = 25°C$		---	450	
				$T_C = 125°C$		---	550	
Turn off time	t_{off}	(See figure 9)		$T_C = -55°C$		---	150	
				$T_C = 25°C$		---	250	
				$T_C = 125°C$		---	400	
Single channel isolation	V_{ISO}	(See figure 10)	f = 1 MHz V_{GEN} = 1 Vp-p	$T_C = 25°C$		50	---	dB
Crosstalk between channels	V_{CT}	(See figure 11)	f = 1 MHz V_{GEN} = 1 Vp-p	$T_C = 25°C$		[illegible]	---	
Charge transfer error	V_{CTE}	(See figure 12)	V_S = GND	$T_C = 25°C$		---	15	mV
Break-before-make time delay	t_D	(See figure 13)		$-55°C \leq T_C \leq 125°C$	03,04, 07	[illegible]	---	ns
Driver input capacitance	C_A	$V_{IN} = 0$ V	(See 4.4.1d)	$T_C = 25°C$	All	---	30	pF
Switch input capacitance	C_{IS}	(See 4.4.1d)	(switch off)	$T_C = 25°C$		---	20	
Switch output capacitance	C_{OS}	(See 4.4.1d)	(switch off)	$T_C = 25°C$		---	20	
Input test voltage	V_{TAP}	C_1 = 100 pF R_2 = 1.5 kΩ	(See 4.5.3)	$T_C = 25°C$		[illegible]	---	V

NOTE:

1. The listed resistance limits correspond to the following voltage values:

75Ω $\pm$9.25 V, $\pm$6.75 V
See table III.
150Ω $\pm$8.50 V, $\pm$6.0 V

Table 4.2 Electrical Parameter Limits /105

Characteristic	Symbol	Conditions $V_{CC} = \pm 15$ V, GND = 0 V Unless otherwise specified	Temperature	Device type	Limits Min	Limits Max	Unit
Drain-source ON resistance	R_{DS}	$V_D = -10$ V, $I_S = 10$ mA See figure 5	$T_A = -55°C$, 25°C $T_A = 125°C$	All All		50 75	Ω 1/
		$V_D = 10$ V, $I_S = -10$ mA See figure 5	$T_A = -55°C$, 25°C $T_A = 125°C$	All All		50 75	
		$V_D = -7.5$ V, $V_{CC} = \pm 10$ V, $I_S = 10$ mA See figure 5	$T_A = -55°C$, 25°C $T_A = 125°C$	All All		70 100	
		$V_{CC} = \pm 10$ V, $V_D = 7.5$ V, $I_S = -10$ mA See figure 5	$T_A = -55°C$, 25°C $T_A = 125°C$	All All		70 100	
Channel ON leakage current	$I_{D(ON)}$	$V_S = V_D = -14$ V (V_{IN} - see 3.4.1) See figure 6	$T_A = -55°C$, 125°C $T_A = 25°C$	All All	-200 -2	200 +2	nA
		$V_S = V_D = +14$ V (V_{IN} - see 3.4.1) See figure 6	$T_A = -55°C$, 125°C $T_A = 25°C$	All All	-100 -1	100 +1	
Drain OFF leakage current	$I_{D(OFF)}$	$V_D = 14$ V, $V_S = -14$ (V_{IN} - see 3.4.1) See figure 9	$T_A = -55°C$, 125°C $T_A = 25°C$	All All	-100 -1	100 +1	
		$V_D = -14$ V, $V_S = 14$ V (V_{IN} - see 3.4.1) See figure 9	$T_A = -55°C$, 125°C $T_A = 25°C$	All All	-100 -1	100 +1	
Source OFF leakage current	$I_{S(OFF)}$	$V_D = 14$ V, $V_S = -14$ (V_{IN} - see 3.4.1) See figure 10	$T_A = -55°C$, 125°C $T_A = 25°C$	All All	-100 -1	100 +1	
		$V_D = -14$ V, $V_S = 14$ V (V_{IN} - see 3.4.1) See figure 10	$T_A = -55°C$, 125°C $T_A = 25°C$	All All	-100 -1	100 +1	
Input current input voltage low	I_{IL}	$V_{IN} = 0$ V See figure 8	$-55°C \le T_A \le 125°C$	All	-1		µA
Input current input voltage high	I_{IH}	$V_{IN} = 5$ V See figure 8	$-55°C \le T_A \le 125°C$	01,02, 03,04	-1		µA
		$V_{IN} = 15$ V See figure 8	$-55°C \le T_A \le 125°C$	All		1	µA
Positive supply current	$+I_{CC}$	$V_{IN} = 0.8$ V See figure 7	$T_A = -55°C$, 25°C	01,02, 03,04		0.01	mA
			$T_A = 125°C$,	01,02, 03,04		0.1	
		$V_{IN} = 4$ V See figure 7	$T_A = -55°C$,	01, 03,04		2.0 2/	
			$T_A = 125°C$, 25°C	01, 03,04		1.0 3/	
		$V_{IN} = 0$ V See figure 7	$T_A = -55°C$, 25°C	05,06, 07,08		0.01	
			$T_A = 125°C$	05,06, 07,08		0.1	
		$V_{IN} = 15$ V See figure 7	$T_A = -55°C$, 25°C	05,06, 07,08		0.01	
			$T_A = 125°C$	05,06, 07,08		0.1	
Negative supply current	$-I_{CC}$	$V_{IN} = 0.8$ V See figure 7	$T_A = -55°C$, 25°C	01,02, 03,04	-0.01		
			$T_A = 125°C$	01,02, 03,04	-0.1		
		$V_{IN} = 4$ V See figure 7	$T_A = -55°C$, 25°C	01,02, 03,04	-0.01		
			$T_A = 125°C$	01,02, 03,04	-0.1		
		$V_{IN} = 0$ V See figure 7	$T_A = -55°C$, 25°C	05,06, 07,08	-0.01		
			$T_A = 125°C$	05,06, 07,08	-0.1		
		$V_{IN} = 15$ V See figure 7	$T_A = -55°C$, 25°C	05,06, 07,08	-0.01		
			$T_A = 125°C$	05,06, 07,08	-0.1		

See footnotes at end of table.

Table 4.2 cont. Electrical Parameter limits /116

Characteristic	Symbol	Conditions V_{CC} = ±15 V, GND = 0 V Unless otherwise specified	Temperature	Device type	Limits Min	Limits Max	Unit
Time to turn ON	t_{ON}	See figure 11	T_A = -55°C	01,02 03,04		260	ns
				05,06 07,08		225	
			T_A = 25°C	01,02 03,04		300	
				05,06 07,08		250	
			T_A = 125°C	01,02 03,04		360	
				05,06 07,08		290	
Time to turn OFF	t_{OFF}	See figure 11	T_A = -55°C	01,02 03,04		230	
				05,06 07,08		140	
			T_A = 25°C	01,02 03,04		250	
				05,06 07,08		150	
			T_A = 125°C	01,02 03,04		290	
				05,06 07,08		160	
Single channel isolation	V_{ISO}	f = 1 MHz See figure 12 V_{GEN} = 1 V_{p-p}	T_A = 25°C	All	50		dB
Crosstalk between channels	V_{CT}	f = 1 MHz See figure 13 V_{GEN} = 1 V_{p-p}	T_A = 25°C	All	50		dB
Charge transfer error	V_{CTE}	V_S = GND See figure 14	T_A = 25°C	All		15	mV
Break-before-make time delay	t_D	See figure 15	-55°C ≤ T_A = ≤125°C	02,04 06,08	20		ns
Driver input capacitance	C_{C1}	V_{IN} = 0 V	T_A = 25°C	All		6	pf
	C_{C2}	V_{IN} = 15 V	T_A = 25°C	All		3.5	
Switch input capacitance	C_{IS}		T_A = 25°C	All		14	pf
Switch output capacitance	C_{OS}		T_A = 25°C	All		14	pf
Input test voltage	V_{ZAP}	C_1 = 100 pf, R_Z = 1.5 k (see 4.5.3)	-55°C ≤ T_A ≤ 125°C	All	400		V

1/ The listed resistance limits correspond to the following voltage values:
9.5 V, -9.5 V ⟶ 50Ω   6.8 v, -6.8 v ⟶ 70Ω
9.25 V, -9.25 V ⟶ 70Ω   6.5 v, -6.5 v ⟶ 100Ω

2/ $+I_{CC}$ = 1.0 mA max for device 02 only.

3/ $+I_{CC}$ = .5 mA max for device 02 only.

Table 4.2 cont. Electrical Parameter Limits /116

Test	Symbol	Conditions V+ = 15 V, GND = 0 V, V- = -15 V unless otherwise specified		Device type	Limits		Unit
					Min	Max	
Switch "ON" resistance (figure 7)	R_{DS}	V_{IN} = 0.8 V, V_S = 10 V, I_D = -1 mA	T_A = -55°C, +25°C	01		70	Ω
			T_A = 125°C			100	Ω
			T_A = -55°C, +25°C	02		175	Ω
			T_A = 125°C			250	Ω
		V+ = 10 V, V- = -10 V, V_{IN} = 0.8 V, V_S = 7.5 V, I_D = -1 mA	T_A = -55°C, +25°C	01		100	Ω
			T_A = 125°C			150	Ω
			T_A = -55°C, +25°C	02		200	Ω
			T_A = 125°C			250	Ω
		V_{IN} = 0.8 V, V_S = -10 V, I_D = 1 mA	T_A = -55°C, +25°C	01		70	Ω
			T_A = 125°C			100	Ω
			T_A = -55°C, +25°C	02		175	Ω
			T_A = 125°C			250	Ω
		V+ = 10 V, V- = -10 V, V_{IN} = 0.8 V, V_S = -7.5 V, I_D = 1 mA	T_A = -55°C, +25°C	01		100	Ω
			T_A = 125°C			150	Ω
			T_A = -55°C, +25°C	02		200	Ω
			T_A = 125°C			250	Ω
Source "OFF" leakage current (figure 8)	$I_{S(OFF)}$	V_S = 14 V, V_D = -14 V, V_{IN} = 2.4 V	T_A = 25°C	01,02	-2	2	nA
			T_A = 125°C		-100	100	nA
			T_A = -55°C		-100	100	nA
		V_S = -14 V, V_D = 14 V, V_{IH} = 2.4 V	T_A = 25°C	01,02	-2	2	nA
			T_A = 125°C		-100	100	nA
			T_A = -55°C		-100	100	nA
Drain "OFF" leakage current (figure 9)	$I_{D(OFF)}$	V_D = -14 V, V_S = 14 V, V_{IN} = 2.4 V	T_A = 25°C	01,02	-2	2	nA
			T_A = 125°C		-100	100	nA
			T_A = -55°C		-100	100	nA
		V_D = 14 V, V_S = -14 V, V_{IN} = 2.4 V	T_A = 25°C	01,02	-2	2	nA
			T_A = 125°C		-100	100	nA
			T_A = -55°C		-100	100	mA

Table 4.2 cont. Electrical Parameter Limits /123

Test	Symbol	Conditions V+ = 15 V, GND = 0 V, V- = -15 V unless otherwise specified		Device type	Limits		Unit
					Min	Max	
Channel "ON" leakage current (figure 10)	$I_{D(ON)}$	$V_D = V_S = 14$ V $V_{IN} = 0.8$ V	T_A = 25°C	01	-2	2	nA
				02	-2	2	nA
			T_A = 125°C	01,02	-200	200	nA
			T_A = -55°C		-200	200	nA
		$V_D = V_S = -14$ V $V_{IN} = 0.8$ V	T_A = 25°C	01	-2	2	nA
				02	-2	2	nA
			T_A = 125°C	01,02	-200	200	nA
			T_A = -55°C		-200	200	nA
Low level input current (figure 11)	I_{IL} 1/	V_{IL} = 0.8 V V_{IH} - 2.4 V	T_A = 25°C	01,02	-0.5	0.5	µA
			T_A = 125°C		-1.0	1.0	µA
			T_A = -55°C		-1.0	1.0	µA
High level input current (figure 11)	I_{IH}	V_{IL} = 0.8 V V_{IN} = 15 V	T_A = 25°C	01,02	-0.5	0.5	µA
			T_A = 125°C		-1.0	1.0	µA
			T_A = -55°C		-1.0	1.0	µA
Supply current (figure 12)	$+I_{CC}$	V_{IL} = 0 V (all inputs)	T_A = 25°C, 125°C	01,02		1.5	mA
			T_A = -55°C			2.0	mA
		V_{IH} = 5 V (all inputs)	T_A = 25°C, 125°C	01,02		1.5	mA
			T_A = -55°C			2.0	mA
Supply current (figure 12)	$-I_{CC}$	V_{IL} = 0 V (all inputs)	T_A = 25°C, 125°C	01,02	-1.5		mA
			T_A = -55°C		-2.0		mA
		V_{IH} = 5 V (all inputs)	T_A = 25°C, 125°C	01,02	-1.5		mA
			T_A = -55°C		-2.0		mA
Capacitance: address	C_A	T_A = 25°C GND = 0 V f = 1 MHz (see 4.4.1c)	V_{IL} = 0 V	01,02		15	pF
Capacitance: input switch	C_{IS}	T_A = 25°C GND = 0 V f = 1 MHz (see 4.4.1c)	V_{IH} = 5 V	01,02		15	pF

1/ Input current at one input node.

Table 4.2 cont. Electrical Parameter Limits /123

Test	Symbol	Conditions V+ = 15 V, GND = 0 V, V- = -15 V unless otherwise specified		Device type	Limits		Unit
					Min	Max	
Capacitance: output switch	C_{OS}	T_A = 25°C GND = 0 V f = 1 MHz (see 4.4.1c)	V_{IH} = 5 V	01,02		20	pF
Off isolation	V_{ISO}	T_A = 25°C; f = 200 kHz, V_{gen} = 1 vp-p (see 4.4.4b)		01,02	60		dB
Crosstalk between channels	V_{CT}	T_A = 25°C, f = 200 kHz, V_{gen} = 1 vp-p (see 4.4.4b)		01,02	60		dB
Charge transfer error	V_{CTE}	T_A = 25°C (see 4.4.4b)		01,02	-10	10	mV
Input test voltage	V_{ZAP}	C_1 = 100 pF, R_2 = 1.5 kΩ (see 4.5.3)		01,02	400		V
Turn "ON" time	$t_{(ON)}$	C_L = 100 pF R_L = 1 kΩ (Figure 13)	T_A = 125°C	01,02		800	ns
			T_A = -55°C, 25°C			600	ns
Turn "OFF" time	$t_{(OFF)}$	C_L = 100 pF R_L = 1 kΩ (Figure 13)	T_A = 125°C	01,02		650	ns
			T_A = -55°C, 25°C			500	ns

Table 4.2 cont. Electrical Parameter Limits /123

in-house electrical characterization procedures were added. These are crosstalk, isolation, charge transfer error, break-before make time delay, driver input capacitance, and switch input and output capacitances. The final list of tests for MIL-M-38510/105, /116 and /123 are shown in table 4.2. The tests for the three specifications are basically the same, and the discussion of devices throughout the remainder of the report will focus on parts covered by MIL-M-38510/116 (300 series). The switches are placed in either the closed "ON" position or the open "OFF" position using the logic inputs voltages (V_{IN}) shown in table 4.3.

TABLE 4.3 INPUT LOGIC THRESHOLDS

DEVICE TYPES	*V_{IN}	SWITCH "ON"	SWITCH "OFF"
01,05	VIL	--	1,2
	VIH	1,2	--
02,06	VIL	2	1
	VIH	1	2
03,07	VIL	--	1,2,3,4
	VIH	1,2,3,4	--
04,08	VIL	3,4	1,2
	VIH	1,2	3,4

*V_{IN}: device types 01-04 VIL≤0.8v ; VIH≥4v
device types 05-08 VIL≤3.5v ; VIL≥11v

4.4 TEST RESULTS AND DISCUSSION

The parameters listed in table 4.2 for MIL-M-38510 /116 were measured using the following test techniques:

Drain-Source ON Resistance (RDS)

Drain to source "ON" resistance RDS is determined by applying a +10mA current to the source and -10V to the drain. The voltage present at the source terminal is measured and RDS is determined using the following equation:

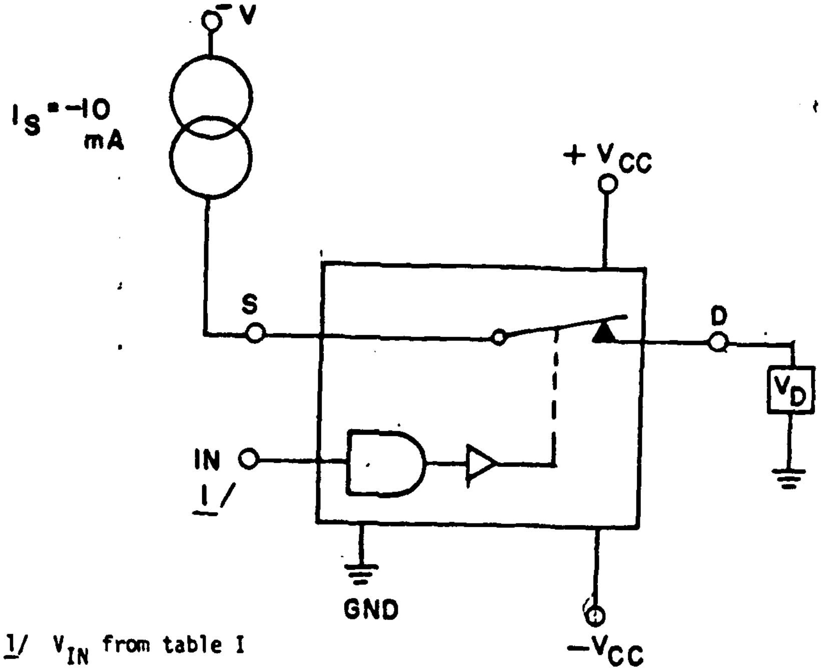
$$RDS = (V_S - V_D)/10mA$$

The test circuit for "ON" resistance is shown in figure 4.2. The test is repeated with a source current of -10mA and a drain voltage of +10V. Each switch within the device is measured.

The variation of "ON" resistance for a closed CMOS switch with respect to voltage variation at the source was examined. The effect was very pronounced when compared to that of a JFET switch under the same conditions. Figure 4.3 displays the switch resistance variation by double humped curves on the graph. It can be seen that the maximum resistance points are generated as the voltages approach the power supply limits (typically 2 to 3 volts less than the supplies). From figure 4.4 it can also be seen that the double humped curves slide upward into increased resistance areas as the power supply voltages drop. As the power supply voltages approach the +/-5V level, the negative analog voltage has a more pronounced effect on the shape of the RDS curve. For this reason RDS "ON" resistance is also tested with the power supply voltages dropped from +/- 15V to +/- 10V and a drain voltage of +/-7.5V (source current remains at +/- 10mA). The effect of increasing temperature can be seen in figure 4.3, therefore testing is also performed at -55C and +125C to verrify the device meets the specified limits.

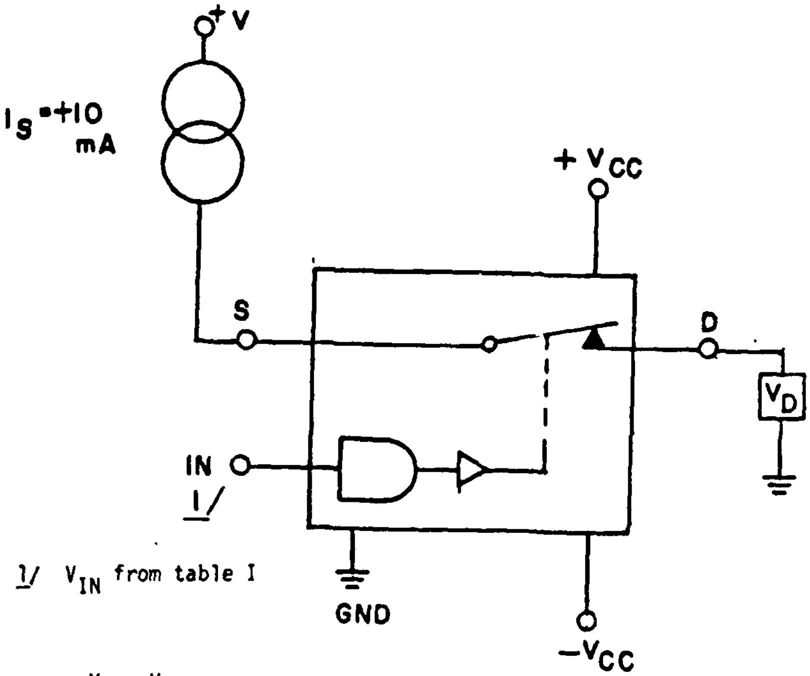
SOURCE "OFF" LEAKAGE CURRENT ($I_{S(OFF)}$)

The test circuit for source "OFF" leakage current is shown in figure 4.5. The proper logic input voltage is applied to maintain the switch in the "OFF" position and, the current flow present at the source is measured with



1/ V_{IN} from table I

$$R_{DS} = \frac{V_S - V_D}{-10\ mA}$$



1/ V_{IN} from table I

$$R_{DS} = \frac{V_S - V_D}{10\ mA}$$

Figure 4.2 R_{DS} Test Circuit

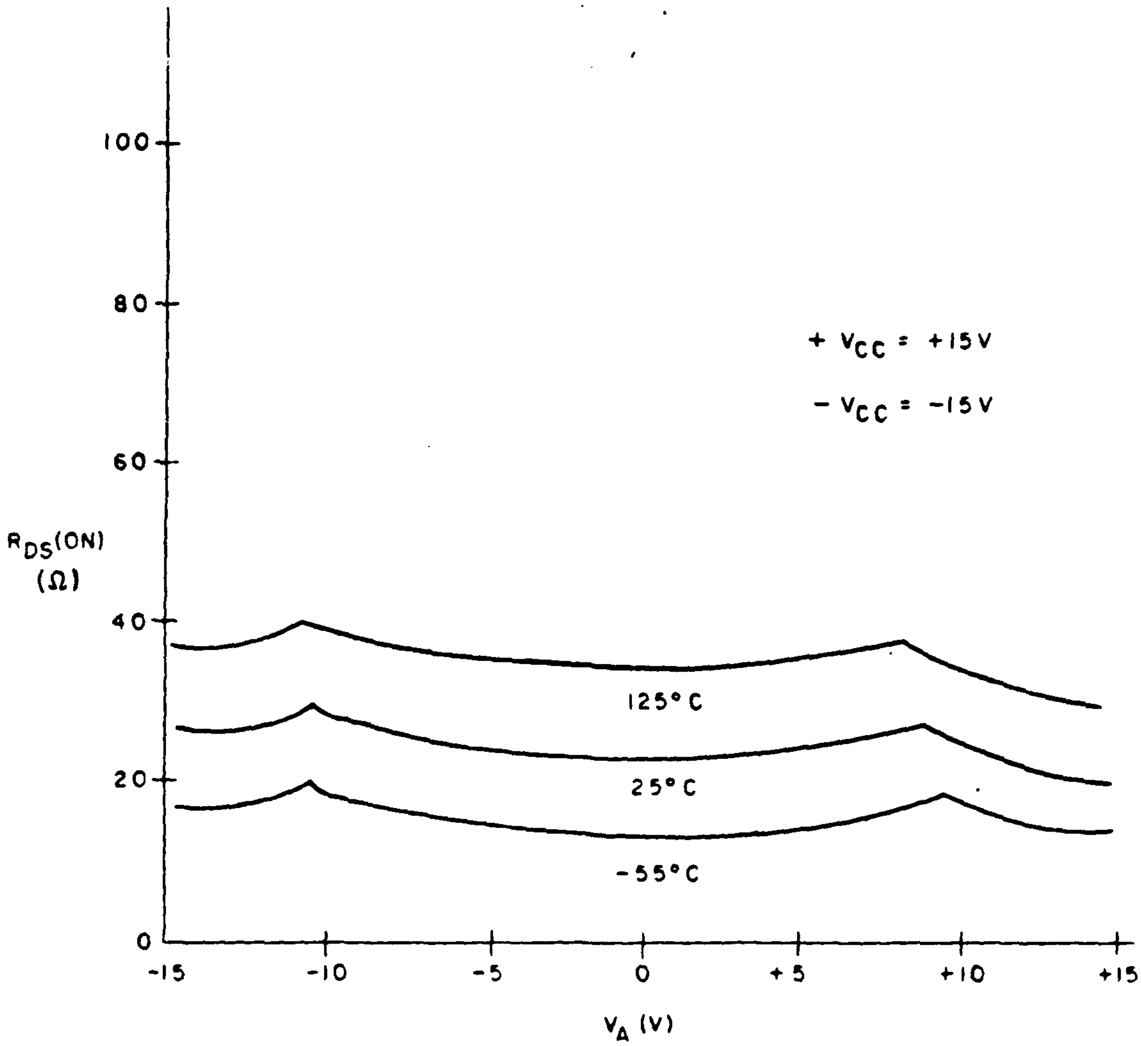


Figure 4.3 $R_{DS(ON)}$ versus V_A and temperature.

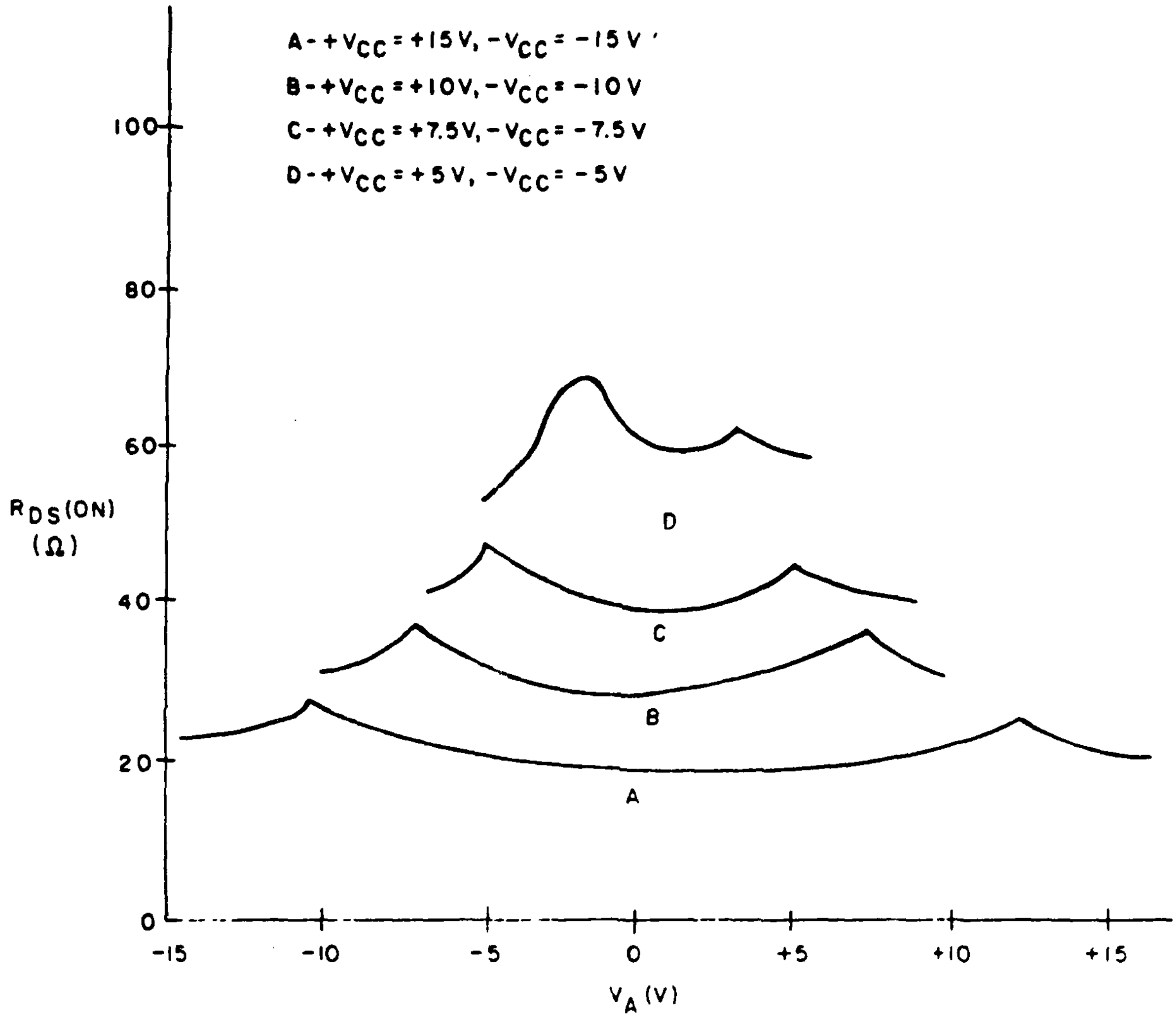
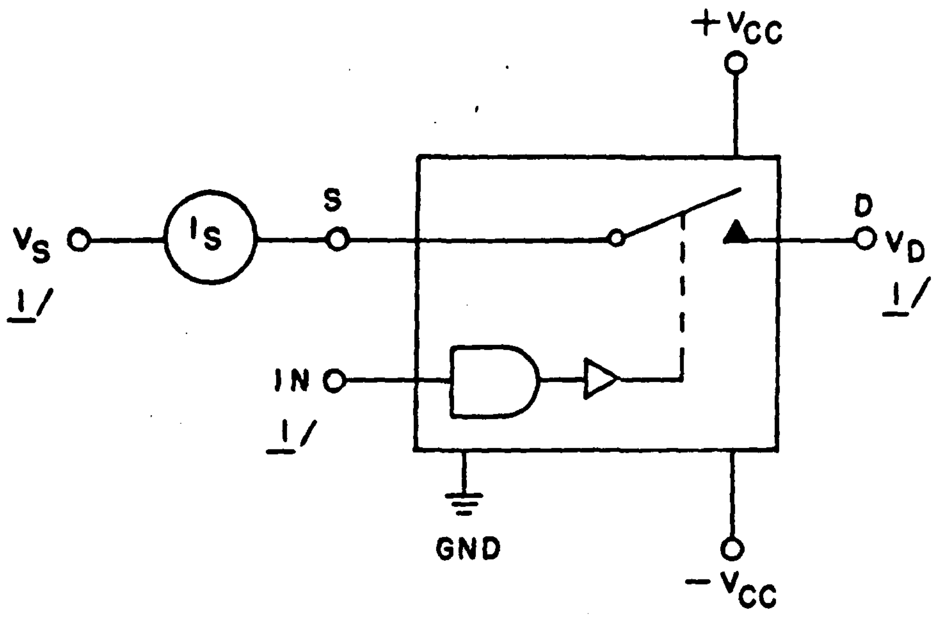


Figure 4.4 $R_{DS(ON)}$ versus V_A and power supply voltage.



1/ Test conditions are from table I.

Figure 4.5 I_S(OFF) Test Circuit

14 volts at the drain and -14 volts at the source. Each switch is placed in the "OFF" position and the current measured. The test is also done with the voltage polarities of the source and drain reversed.

DRAIN "OFF" LEAKAGE CURRENT ($I_{D(OFF)}$)

The drain "OFF" leakage current is determined in the same manner as I S(OFF) currentdescribed above. The only difference is the amount of current present at the drain terminal in the "OFF" switch is measured. The test circuit is pictured in figure 4.6 .

CHANNEL "ON" LEAKAGE CURRENT ($I_{D(ON)}$)

The circuit used to determine channel "ON" current is shown in figure 4.7. The figure shows the source and drain are connected together. The current into the sourced-drain combination is measured first with a voltage of -14V applied to source and drain. The measurement is repeated with +14V applied. The logic input voltage is such that the switches are placed in the "ON" position.

INPUT VOLTAGE, HIGH AND LOW CURRENT (I_{IH}, I_{IL})

Input voltage high current, I_{IH}, is measured at the logic input terminal with the source and the drain open. The current flow present is determined with V_{IN} set to 15 volts for device types 01-08 and repeated for V_{IN} set to 5 volts for device types 01-04. The input voltage low current I_{IL} is measured with Vin set to 0 volts. The test circuit is shown in figure 4.8.

POSITIVE AND NEGATIVE SUPPLY CURRENT ($+I_{CC}$, $-I_{CC}$)

The circuit used for testing is pictured in figure 4.9. The amount of current at the positive and negative supply terminals is measured with the

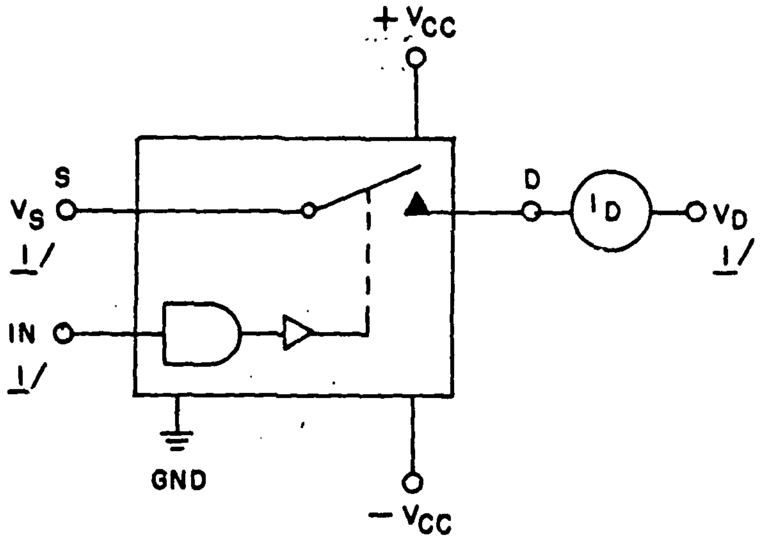
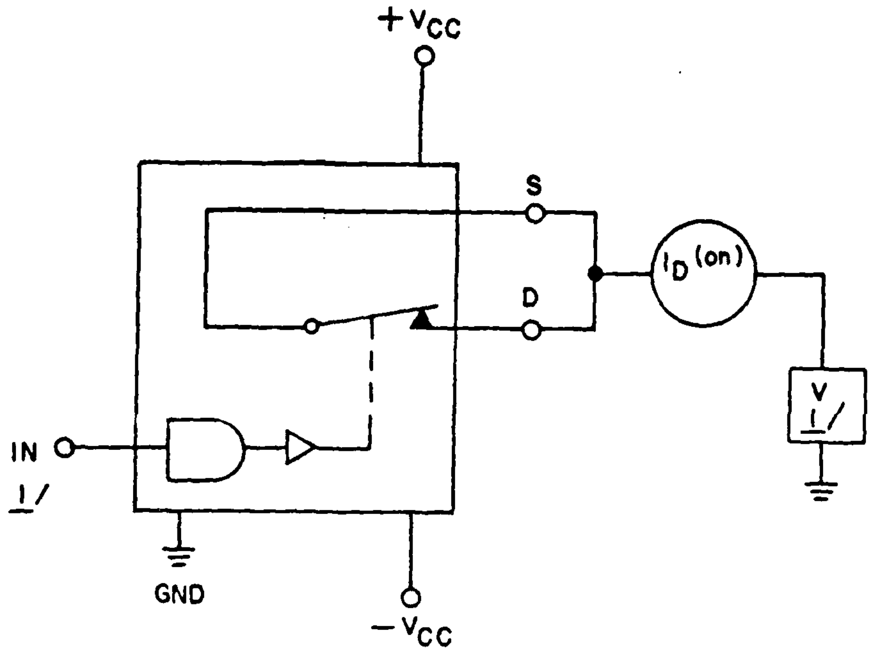


Figure 4.6 I_D(OFF) Test Circuit



1/ Test conditions are from table I

Figure 4.7 I_D(ON) Test Circuit

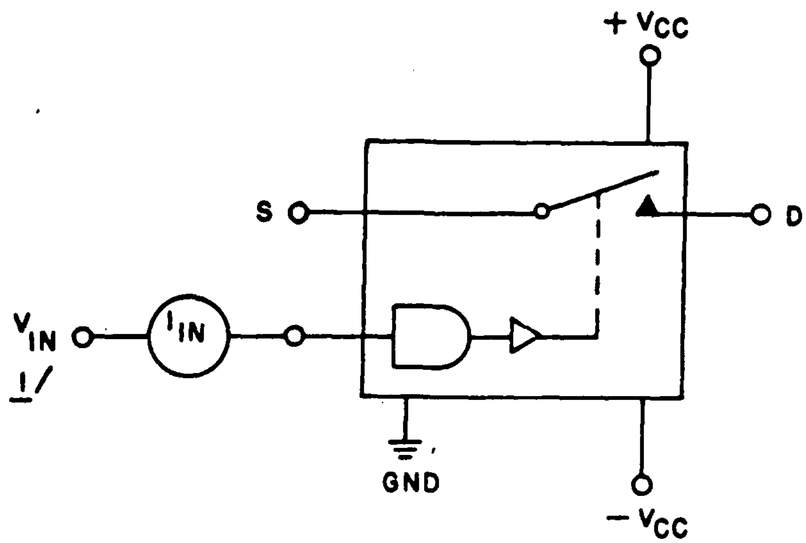
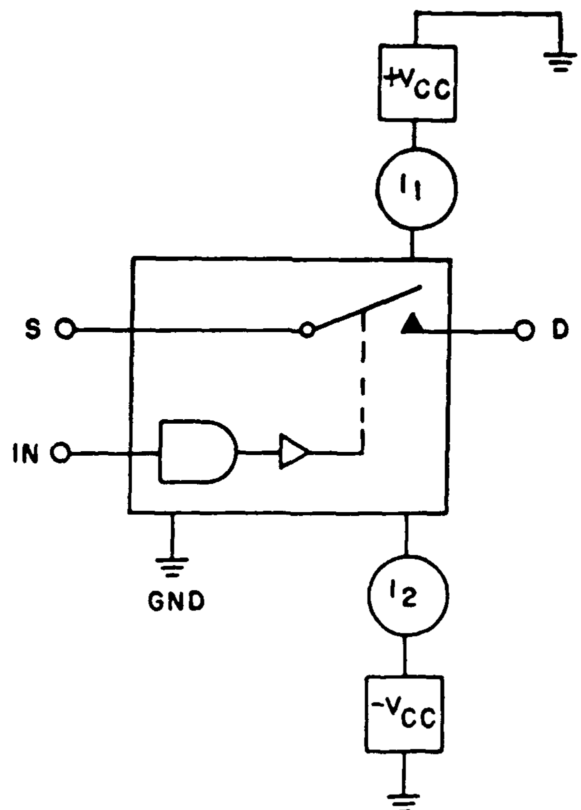


Figure 4.8 I_{IH},I_{IL} Test Circuit



1/ Test conditions are from table I.

Figure 4.9 $\pm I_{CC}$ Test Circuit

power supply voltage set to +15 and -15 volts, respectively. The test are performed with various logic input voltages shown in table 4.2.

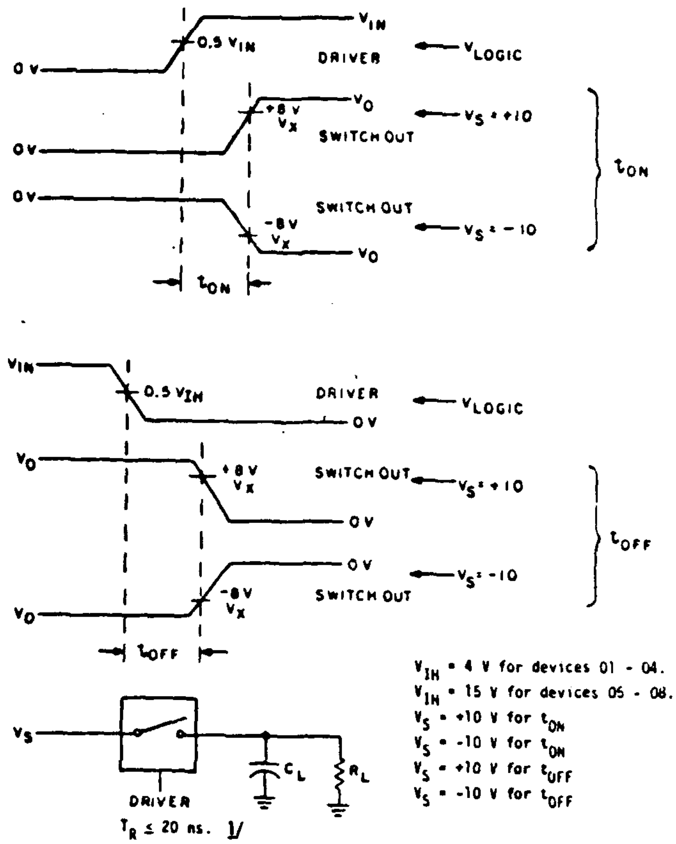
TURN "ON" , TURN "OFF" TIME (t_{ON}, t_{OFF})

In ordc, to make the waveforms repeatable, a capacitor and resistor are specified for a load on the drain (CL=100pF includes jig, probe and stray capacitance, and RL=1Kohms). For both the t_{ON} and t_{OFF}, measurements are taken with the source first set to +10 volts, and then -10 volts. The logic input waveform required to perform this test is shown in figure 4.10. The "ON" time is measured from the 50% point of V_{IN} to the 80% point of Vs; this is also true for the "OFF" time. The 80% point was chosen due to capacitance problems. If the 90% point is selected for the t_{OFF} measurement, automatic test equipment (ATE) will measure the first downslope of the initial dip which will not represent the proper turn-off time. This would allow t_{OFF} to appear better than it actually is. The solution is to select a voltage measurement value further down the curve and away from the spiking situation. In the process of doing this, however, a trade off must be made as to how much of a capacitive tail will be acceptable. Thus, for the purpose of ATE compatibility, measurements are made as high on the curve as possible and still be a sufficient amount away from the problem area. For these device types a voltage point of 80% was chosen.

SINGLE CHANNEL ISOLATION (V_{ISO})

The test circuit is shown in figure 4.11. The amount of isolation afforded by the switch in the "OFF" state is measured by appling a 1 volt peak to peak, 1 MHz sinewave to the source and determining the voltage present across a 1K ohm local resistor connected to the drain. The isolation (V_{ISO}) in dB is determined using the following equation:

$$V_{ISO} = - 20\log (V_D/V_S)$$



R_L = 1 kΩ ±5%.

C_L = 100 pf ±5% (includes test and jig capacitance).

NOTES:

1. The logic driver shall have the following characteristics:

   a. V_{LOGIC} = 0 V to +4 V for parts 01 - 04.
      V_{LOGIC} = 0 V to +15 V for parts 05 - 08.

   b. Rise time (0.4 V to 3.6 V) ≤ 10 ns
      Fall time (3.6 V to 0.4 V) ≤ 10 ns } Part types 01 - 04

      Rise time (1.5 V to 13.5 V) ≤ 20 ns
      Fall time (13.5 V to 1.5 V) ≤ 20 ns } Part types 05 - 08

2. See 3.4.1 for appropriate switching conditions.
3. V_{SOURCE} (V_S) = +10 V and -10 V for t_{ON}.
   V_{SOURCE} (V_S) = +10 V and -10 V for t_{OFF}.
4. V_X = +8 V for +10 V condition in note 3 above.
   V_X = -8 V for -10 V condition in note 3 above.

Figure 4.10 Input-output waveform for time delay test

CROSSTALK BETWEEN CHANNELS (V_{CT})

The setup for load resistors and switch positions for this test is shown in figure 4.12. Crosstalk determines the amount of signal present on the drain of an open switch due to a signal on a closed switch. Apply a 1V p-p, 1MHz sine wave to the source of the "ON" switch and measure the signal at the drain of the "OFF" switch V_{CT} in dB is found by the following equation:

$$V_{CT} = -20 \log (V_D/V_S)$$

CHARGE TRANSFER ERROR (V_{CTE})

Charge transfer error indicates the amount of signal present at the drain of an "OFF" switch due to a signal on the logic input terminal. The test circuit input and output waveforms are shown in figure 4.13. A 0.01uF capacitor is placed on each drain and a 1Khz square wave (tr<=20ns) with a voltage swing of 0 to 4 volts for device types 01-04 (0 to 15 for device types 05-08) applied to the logic input terminal. The measurement is made on the drain terminal as shown in figure 4.13.

BREAK-BEFORE-MAKE TIME DELAY (t_D)

The test circuit and waveforms are shown in figure 4.14. A load resistor (RL=1Kohms) and a load capacitor (Cl= 100pF) are used on the drains to maintain a consistent measurement. As can be seen from the figure the sources are tied first to +10 volts then to -10 volts and the drains are connected to the load. The test is only performed on device types 02,04,06 and 08. The voltage and timing requirements of the logic input signal as well as the measurement points for t_D are pictured in the figure. The break-before make time delay was questionable at -55C for JFET analog switches. This is not the case with CMOS switches; they exhibit a fairly constant time delay over the military temperature range. Therefore t_D is only sample tested at -55C.

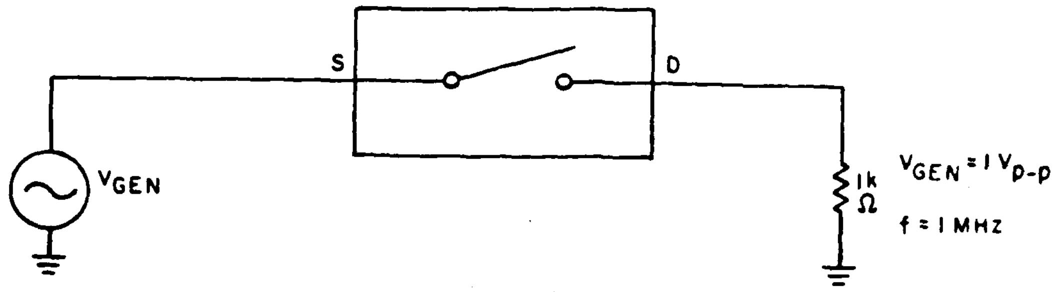


Figure 4.11 Isolation test circuit.

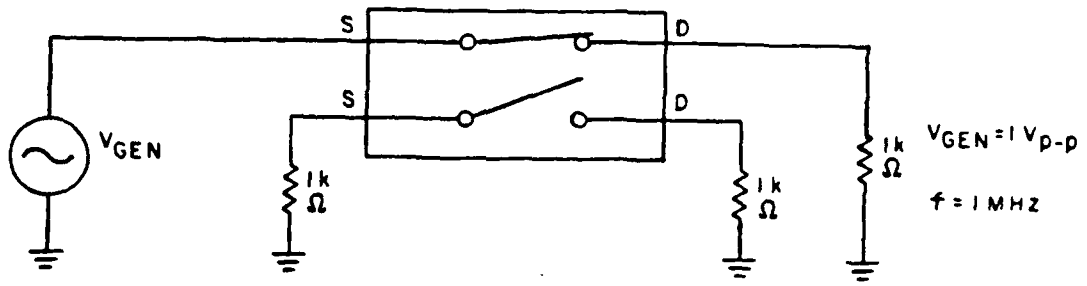


Figure 4.12 Crosstalk test circuit.

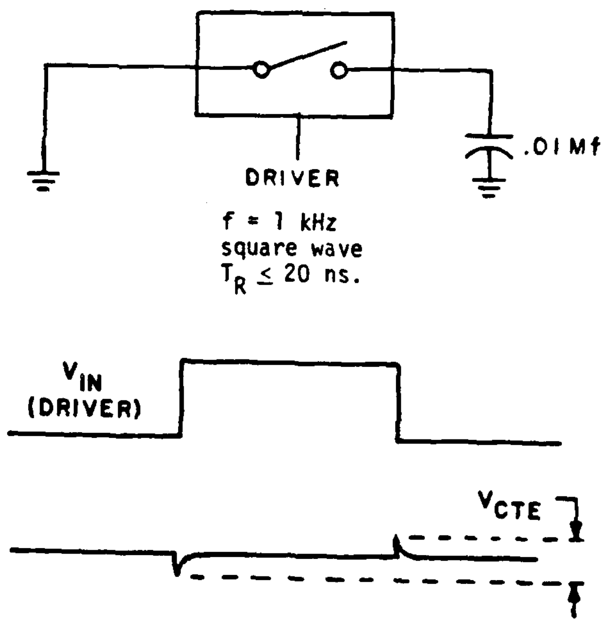
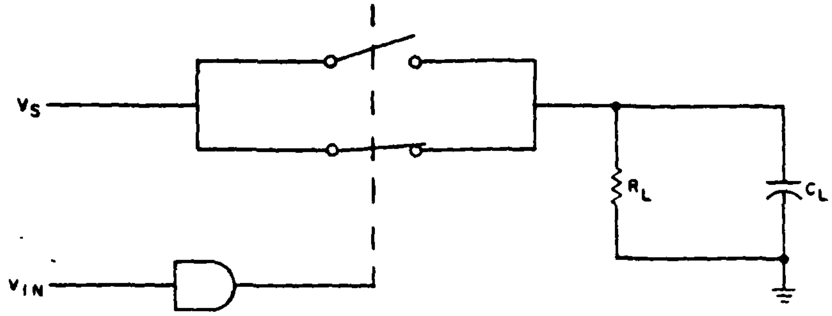
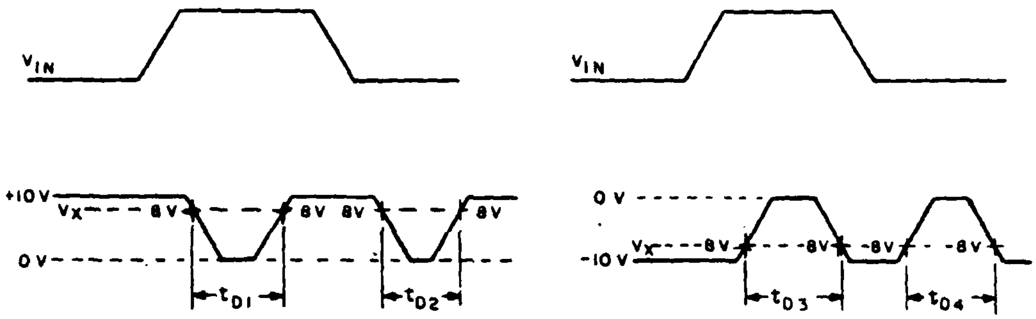


Figure 4.13 Charge transfer error test circuit.





CONDITION A

CONDITION B

NOTES:

1. R_L = 1 kΩ ±5%, C_L = 100 pf ±5%.
2. T_{D1}, T_{D2}, T_{D3} and T_{D4} shall all be measured. These measurements shall apply only to device types 02, 04, 06, and 08. See 3.4.1 for switch conditions.
3. V_{SOURCE} (V_S) = +10 V for condition A (all part types).
   V_{SOURCE} (V_S) = -10 V for condition B (all part types).
4. V_X = +8 V for condition A (all part types).
   V_X = -8 V for condition B (all part types).
5. The logic driver shall have the following characteristics:
   a. V_{LOGIC} = 0 V to +4 V for part types 01 - 04.
      V_{LOGIC} = 0 V to +15 V for part types 05 - 08.
   b. Rise time (0.4 V to 3.6 V) ≤ 10 ns
      Fall time (3.6 V to 0.4 V) ≤ 10 ns } Part types 01 - 04

      Rise time (1.5 V to 13.5 V) ≤ 20 ns
      Fall time (13.5 V to 1.5 V) ≤ 20 ns } Part types 05 - 08

Figure 4.14 Break-Before-Make Test Circuit

SWITCH CAPACITANCE ($C_{C1}, C_{C2}, C_{IS}, C_{OS}$)

The capacitance parameters tested involved driver input (C_{C1}, C_{C2}), switch input (C_{IS}) and switch output (C_{OS}) capacitances. They supply design engineers with necessary information when using the devices in interface applications. The test procedures for measuring these capacitance values are listed in test method 3012.1 of MIL-STD-883. Since the measured values are primarily a function of the fabrication process, the tests are only required for initial qualification and for process changes which affect these values.

4.5 CONCLUSION AND RECOMENDATIONS

Burn-in techniques have also been investigated for the CMOS switch technology. The complexity of the CMOS analog switch family is far less than that of the JFET switch series covered under MIL-M-38510/105, /116, and /123. The device types do not contain multiple technologies, nor are multi-chip or hybrid considerations involved since the devices are strictly monolithic. However, an in-house investigation relating to burn-in techniques was conducted with the results documented in the MIL-M38510/116 detail specification. The circuit shown in the specification are the recommended burn-in circuits. Both JFET and CMOS categories have static, dynamic, and accelerated options available. Requirements directing the use of the options regarding qualification of devices for Classes B and S are documented in the respective detail specifications.

The problem of "ON" resistance variation with analog voltage was discussed at JC-41. Although RADC verified this phenomenon exists, it was determined that the process variations are such that maintenance of process control to obtain the specified electrical limits would be impractical if not impossible. It was decided, however, that inclusion in the detail specification as a design guide would be in the best military interest. All limits determined to be accurate and reasonable by RADC in-house characterization efforts are fully discussed and coordinated at JC-41 meetings.

4.6 BIBLIOGRAPHY

1. Harris Analog Book (1982)

2. Intersil "Hot Ideas In CMOS" Data Book (1983/1984)

3. Siliconix Integrated Circuits Data Book (1985)

SECTION V

ANALOG MULTIPLEXERS

MIL-M-38510/190

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

5.1 Introduction

This section of the report deals with the characterizaton of CMOS analog multiplexers/demultiplexers. This device family is very similar to the CMOS analog switch family. The testing philosophy is the same, however test implementation differs due to the different function of the microcircuits. Table 5.1 lists the analog multiplexer/demultiplexer specified for MIL-M-38510/190C.

Table 5.1 Device Types Specified

Device	Generic	Manufacture	Description
01	506,6116	S,I	Single 16-channel MUX/DEMUX
02	506A	H	Single 16-channel MUX/DEMUX with overvoltage protection
03	507,6216	S,I	Differential 8-channel MUX/DEMUX
04	507A	H	Differential 8-channel MUX/DEMUX with overvoltage protection
05	508A	H	Single 8-channel MUX/DEMUX with overvoltage protection
06	509A	H	Differential 4-channel MUX/DEMUX with overvoltage protection
07	508,6108	S,I	Single 8-channel MUX/DEMUX
08	509,6208	S,I	Differential 4-channel MUX/DEMUX

Manufacturer code S-Siliconix I-Intersil H-Harris

5.2 Description of Device Types

The analog multiplexers/demultiplexers covered under MIL-M-38510/190C consist of both single and differential types, with or without overvoltage protection. The functional diagrams for device types 01-08 are shown in figure 5.1. The overvoltage protected device types (02,04,05 and 06) are capable of withstanding a continuous voltage on any input of +/- 20 volts greater than the supply voltages. This protection circuitry should enable the device to withstand signal line surges from other power supplies as well as electro static transients.

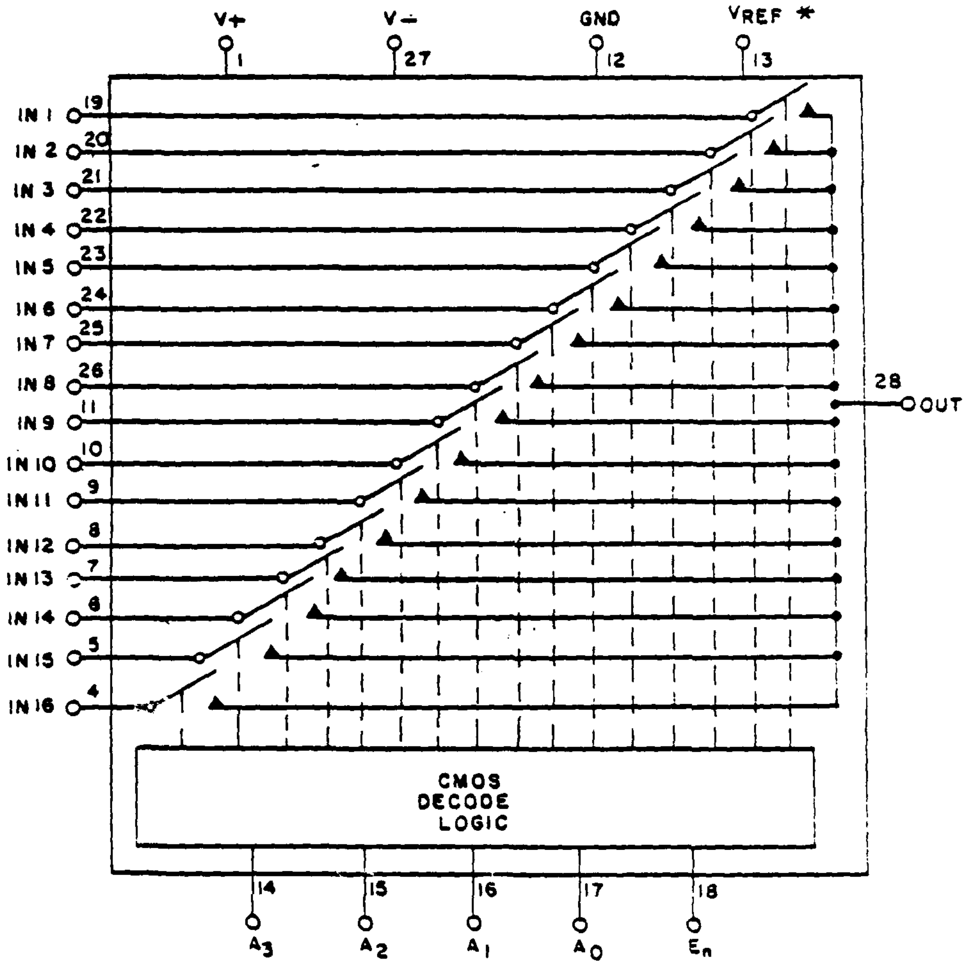
5.3 Test Development

The analog multiplexer chip can be basically divided into two building blocks, the analog switches and the address logic. The function of both of these blocks can be tested simultaneously if one considers the device as 16 separate switches with all the outputs tied together. The only restriction is that only one switch can be on at a time. Using this model it is possible to measure the parameters listed in table 5.2 (see appendix). Switch "ON" resistances and leakage currents for all the channels are two of the tests. Since each switch is addressed for the aforementioned tests, the decoding logic has been concurrently checked. The truth table for the logic is shown in table 5.3. Specifically, the device would fail the RDS test should the improper input be addressed.

It was decided for the implementation of the switching time tests (T_{ON} and T_{OFF})that only switch 1 and switch 16 would be checked. These switches correspond to an address input logic of all "zeros" or all "ones" (If the device is an eight bit mux, switches 1 and 8 would be used). This is the worst case condition since all of the address lines have to change.

As one would suspect, the break-before-make test is very important. It has direct impact on application (one would not want two of the inputs shorted together). This test can be visualized by superimposing the turning ON of switch 1 and the turning OFF of switch 16, and visa versa. The

Device types 01 and 02



* OPTIONAL (NORMALLY LEFT OPEN)

Figure 5.1 Functional diagrams.

Device types 03 and 04

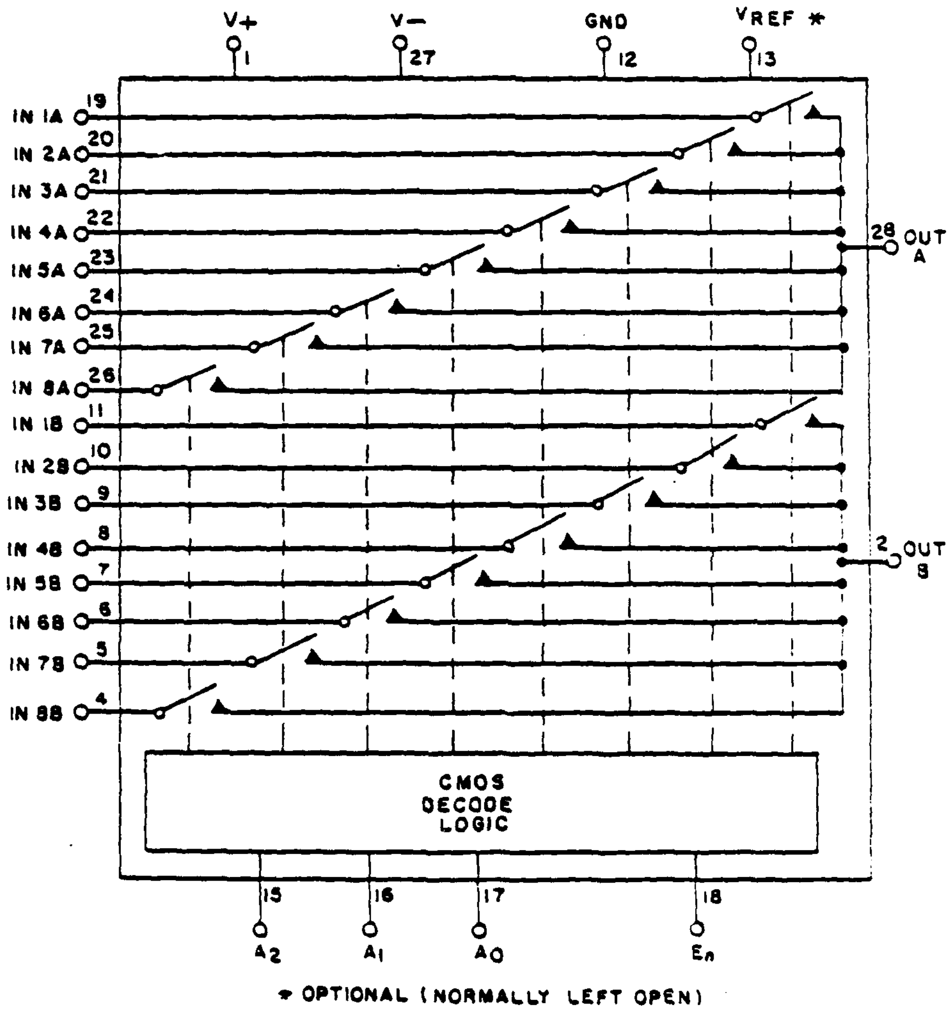
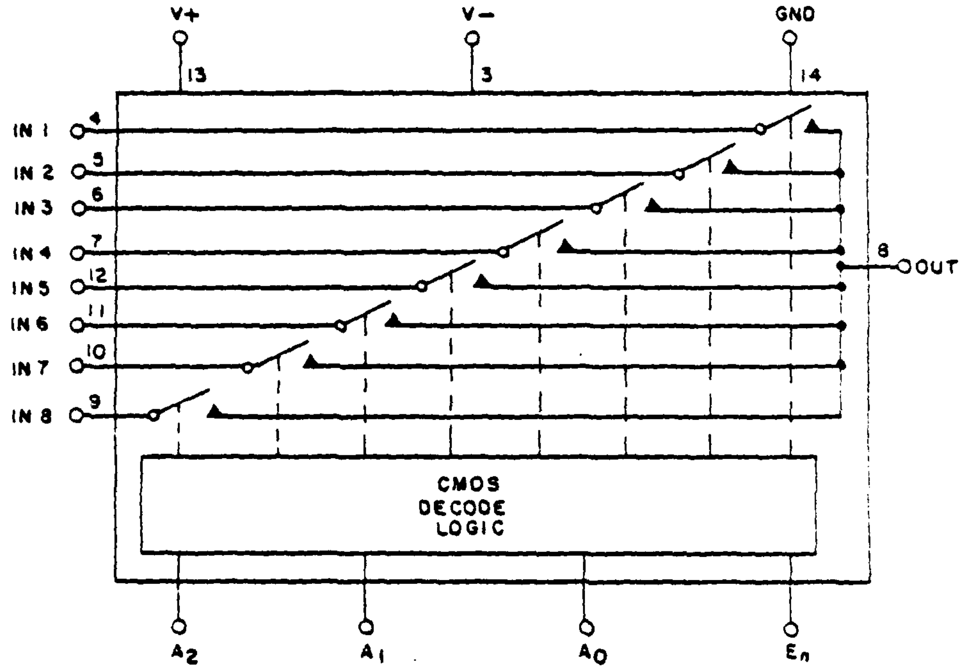


Figure 5.1 Functional diagrams - Continued.

Device types 05 and 07



Device types 06 and 08

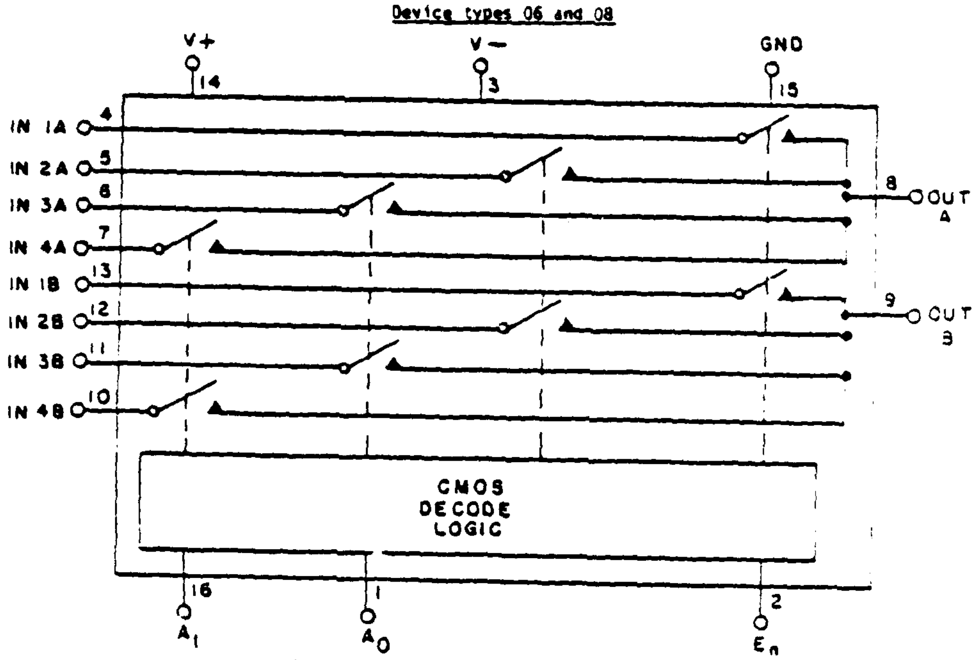


Figure 5.1 Functional diagrams - Continued.

Device types 01 and 02

A3	A2	A1	A0	EN	CHANNEL SELECTED
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

Device types 03 and 04

A2	A1	A0	EN	CHANNEL SELECTED
X	X	X	L	NONE
L	L	L	H	1A,1B
L	L	H	H	2A,2B
L	H	L	H	3A,3B
L	H	H	H	4A,4B
H	L	L	H	5A,5B
H	L	H	H	6A,6B
H	H	L	H	7A,7B
H	H	H	H	8A,8B

Device types 05 and 07

A2	A1	A0	EN	CHANNEL SELECTED
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Device types 06 and 08

A1	A0	EN	CHANNEL SELECTED
X	X	L	NONE
L	L	H	1A,1B
L	H	H	2A,2B
H	L	H	3A,3B
H	H	H	4A,4B

Table 5.3 Truth tables.

break-before-make test is preformed at -55oC on a sample basis. It is interesting to note that both a plus and minus analog voltage is tested for all CMOS switches.

Another switching time associated with the analog multiplexer is the chip enable. This parameter is tested by pulsing the enable pin with the address and input voltage present. By monitoring the output, both the functionality and speed of this parameter is checked.

The device testing was primarily performed with an in-house Tektronix S-3270 Automatic Test System (ATE). Special bench test set-ups were developed to handle selected tests which could not be implemented on ATE equipment due to tester limitations. Parameters tested by bench set-up were the following: crosstalk, isolation and break-before-make.

5.4 Test Results and Discussion

The parameters listed table 5.2 (see appendix) were measured by the following techniques:

Input Clamping Voltage (V_{ICPOS}, V_{ICNEG})

The test is only performed on the device types with overvoltage protection (02,04,05 and 06). For V_{ICPOS}, 1mA is applied to the enable pin and measure the voltage generated at the enable pin is measured. The same test is also performed on all of the logic inputs. The V_{ICNEG} test is measured in the same manner except -1mA is applied to the enable and logic pins.

Input Leakage Current (I_{IH} and I_{IL})

High level input leakage current I_{IH} is determined by applying 4.0 volts sequentially to each address input and measuring the current flow into the

device. Each address input as well as the enable are measured with all unused inputs grounded. Low level input current I_{IL} is measured in the same manner as I_{IH} with the exception that 0.8 volts is applied sequentially to each address input and all unused address inputs are tied to 5 volts

Source OFF leakage Current ($I_{S(OFF)}$)

Source OFF leakage current is the amount of current flow into a switch in the open position. The $I_{S(OFF)}$ measurement is performed by applying 0.8 volts to the enable pin and +10 volts to the source being measured. All remaining unused sources as well as the drain(s) are connected to -10 volts. Measure the current flow into each OFF source sequentially. The test is also performed with -10 volts on the mesured source and +10 volts on the remaining sources and drain(s).

Drain OFF Leakage Current ($I_{D+(OFF)}$,$I_{D-(OFF)}$)

The drain OFF leakage current is the amount of current flow present in the drain while the switch is in the open position. The $I_{D+(OFF)}$parameter is determined by appling +10 volts to the drain(s), 0.8 volts to the enable, -10v to the sources and measuring the current flow out of the drain. For $I_{D-(OFF)}$ thevoltage on the sources and drain are reversed and the current flow at the drain(s) is again measured.

Drain ON Leakage Current ($I_{D(ON)}$)

The ON leakage current is the amount of current flow into the drain while the switch is in the ON (closed) state. For $I_{D(ON)}$ connect the drain and each of the sources sequentially to 10 volts, with all unused sources connected to -10 volts. Measure the current flow present at the drain as each switch is closed. The current at the drain is also measured with -10 volts applied to the drain and active source and +10 volts applied to all unused sources.

Overvoltage Protection Drain OFF Leakage Current ($I_{D(OFF)\ overvoltage}$)

33 volts are sequentially applied to the sources and 0 volts to the drain(s) for $I_{D+(OFF)overvoltage}$. The amount of current is measured at the drain with the enable pin at 0.8 volts (this forces all switches into the opened state). The test is repeated for $I_{D-(OFF)overvoltage}$ with the sources at -33 volts.

Positive and Negative Supply currents (I+,I-)

The positive and negative supply currents are measured by appling 0 volts to the address lines and +5 volts to the enable pin. The power supplies are set to +15 and -15 volts and all other terminals are disconnected.

Standby Positive and Negative Supply Currents (I_{+SBY},I_{-SBY})

The standby current is determined by applying 0 volts to the address and enable pins, +15 volts to V+, and -15 volts to V-. The amount of current in the V+ and V- terminals is measured to obtain I_{+SBY} and I_{-SBY}.

Enable, Address, Output and Input Switch Capacitance (C_{EN},C_A,C_{OS},C_{IS})

The power supplies V+ and V- are set to 0 volts for all capacitance measurements. The test is performed by measuring the capacitance between the terminal of interest and ground using a capacitance bridge with a 1 MHz sinewave. The following symbols are used for capacitance:

C_{EN} - capacitance between the enable pin and ground.
C_A - capacitance between the address lines and ground.
C_{OS} - capacitance between the output(s) (drain) and ground.
C_{IS} - capacitance between the inputs (sources) and ground.

Switch ON Resistance (RDS1,RDS2)

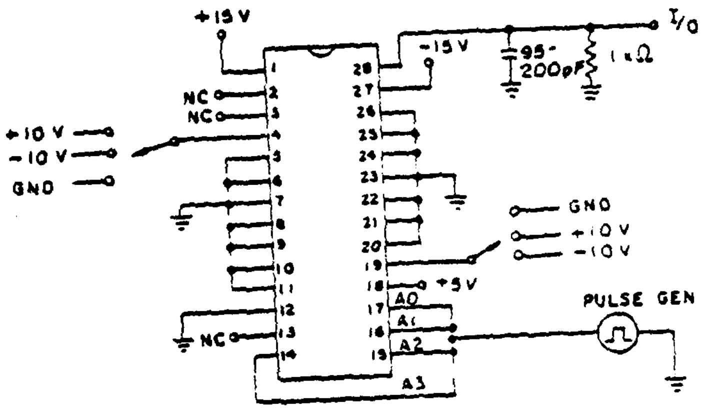
The ON resistance RDS1 is determined by placing 10 volts on each source sequentially and forcing 1mA into the drain for device types 01,03 07 and 08 (100uA for device types 02-06). The address logic is stimulated with the values shown in table 5.3 to activate each switch in turn, and the voltage drop between the active source and drain is measured. The resistance is the amount of voltage dropped, divided by the current at the drain. The measurement is also performed with the source voltage equal to -10 volts and the drain current at -1mA for device type 01,03,07 and 08, and -100uA for the remaining devices.

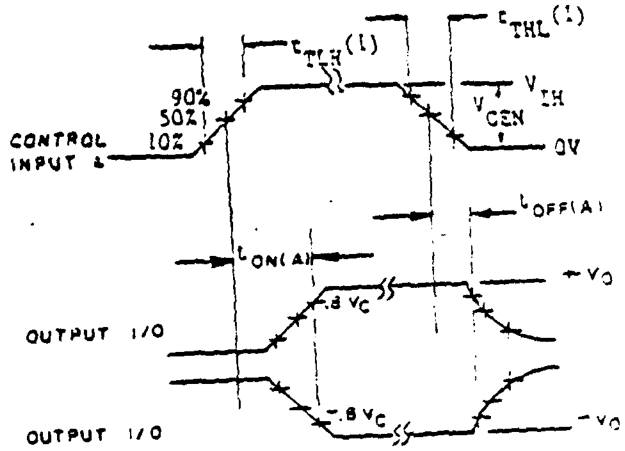
The ON resistance RDS2 is determined in the same manner as RDS1, however the power supplies are lowered from +/-15 volts to +/-10 volts with +7.5 volts applied to the source terminals. The drain currents are 1mA and 100uA as defined for the above device types. The measurement is also performed with the source voltage at -7.5 volts.

Propagation Delay Times: Address Input to I/O ($t_{ON(A)}$,$t_{OFF(A)}$)

A typical test circuit for device types 01 and 02 is shown in figure 5.2. The circuits for the other device types are very similar and will not be shown. The only difference is the number of sources (inputs) and drain(s) (outputs). A load resistor of 1Kohm and a capacitor in the range of 95-200pf (large range is needed for ATE equipment) are connected to the output(s). The address lines are connected to a signal source suppling a +4 volt pulse with transition times less than 20ns. For device types 01 and 02, switches 1 and 16 are used for the test (switches 1 and 8 are used for device types 03,04,05 and 07 and switches 1 and 4 for device types 06 and 08). For testing, switch 1 is set to -10 volts, switch 16 is set to ground, and all remaining switches are grounded. A pulse is applied to the address lines and the output pulse is recorded. As can be seen from figure 5.2, $t_{ON(A)}$ is measured from the 50% point of the input to the 80% of Vc point of the output (Vc is the peak output voltage). The measurement for $t_{OFF(A)}$ is performed from the 50% point of the falling edge of the input to the 80% of Vc point of

Device types 01 and 02





Input pulse requirements:
$V_{GEN} = 4V$
$t_{THL(1)} = t_{TLH(1)} \leq 20$ ns.

DYNAMIC TEST WAVEFORMS

Figure 5.2 Switching times test circuit and waveforms.
(Address inputs to I/O)

the output. Further testing is performed with the switch voltages reversed, that is switch 1 is grounded and 16 is at -10 volts. All other switches are grounded.

Propagation Delay Times: Enable to I/O ($t_{ON(EN)}$,$t_{OFF(EN)}$)

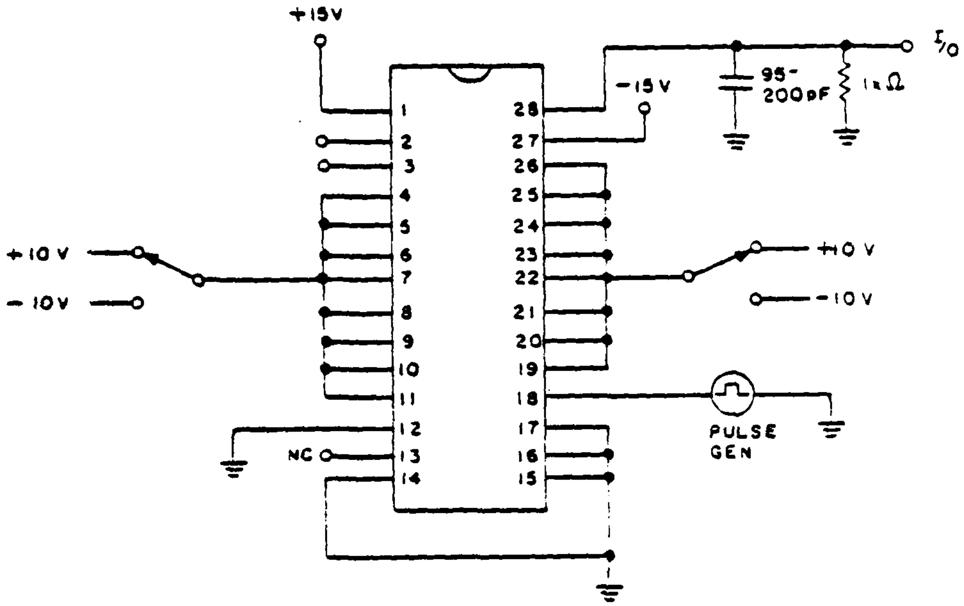
As in the previous delay time measurement the output load consists of a 1Kohm resistor and 95 to 200pf capacitor. The address lines are connected to ground and a pulse is applied to the enable pin using a signal generator, V_{GEN} at+4V, and rise and fall times < 20nS. Two iterations of $t_{ON(EN)}$ and $t_{OFF(EN)}$ areperformed. The first is with +10 volts connected to all of the switch inputs, the second is with -10 volts connected. The test circuit for the enable to I/O propagation delay is shown in figure 5.3. The input and output waveforms are shown and it can clearly be seen that $t_{ON(EN)}$ measurementis from the 50% point of V_{GEN} to the 0.8Vc point of the output. The $t_{OFF(EN)}$ measurement is performed at the same points only on the falling edge of the output (10 to 0 volt transistion).

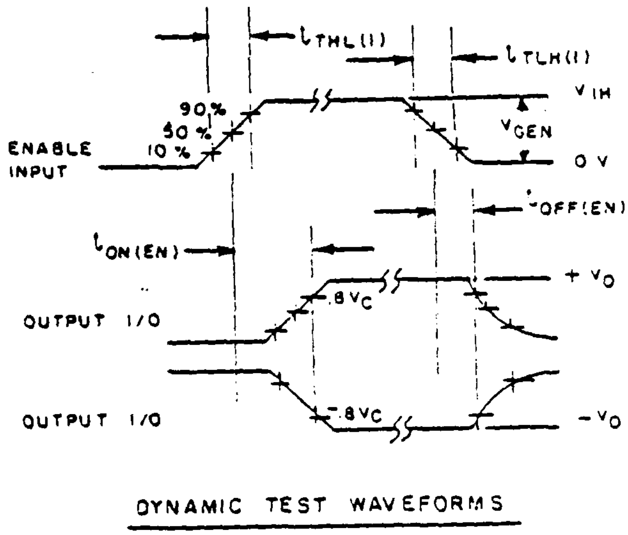
Break-Before-Make Time Delay (t_D)

For the break-before-make time delay all of the inputs of the device are connected to +10 volts with the address lines connected to a +4 volt pulse generated with transition times less than 20 nS. The output(s) have a 1Kohm load resistor as well as a 95-200pf load capacitor. Since the inputs are at the same potential, the output waveform will contain a small glitch when the address lines are pulsed; this is the break-before- make delay. The test circuit and waveform are shown in figure 5.4. The delay time is measured at the 90% point from ground, and insures a uniform reference point. The testing is repeated with -10 volts connected to the inputs.

Single Channel Isolation (V_{ISO})

Device types 01 and 02





Input pulse requirements:
$V_{GEN} = 4$ V.
$t_{THL(1)} = t_{TLH(1)} \leq 20$ ns.

Figure 5.3 Switching times test circuit and waveforms.
(Enable to I/O)

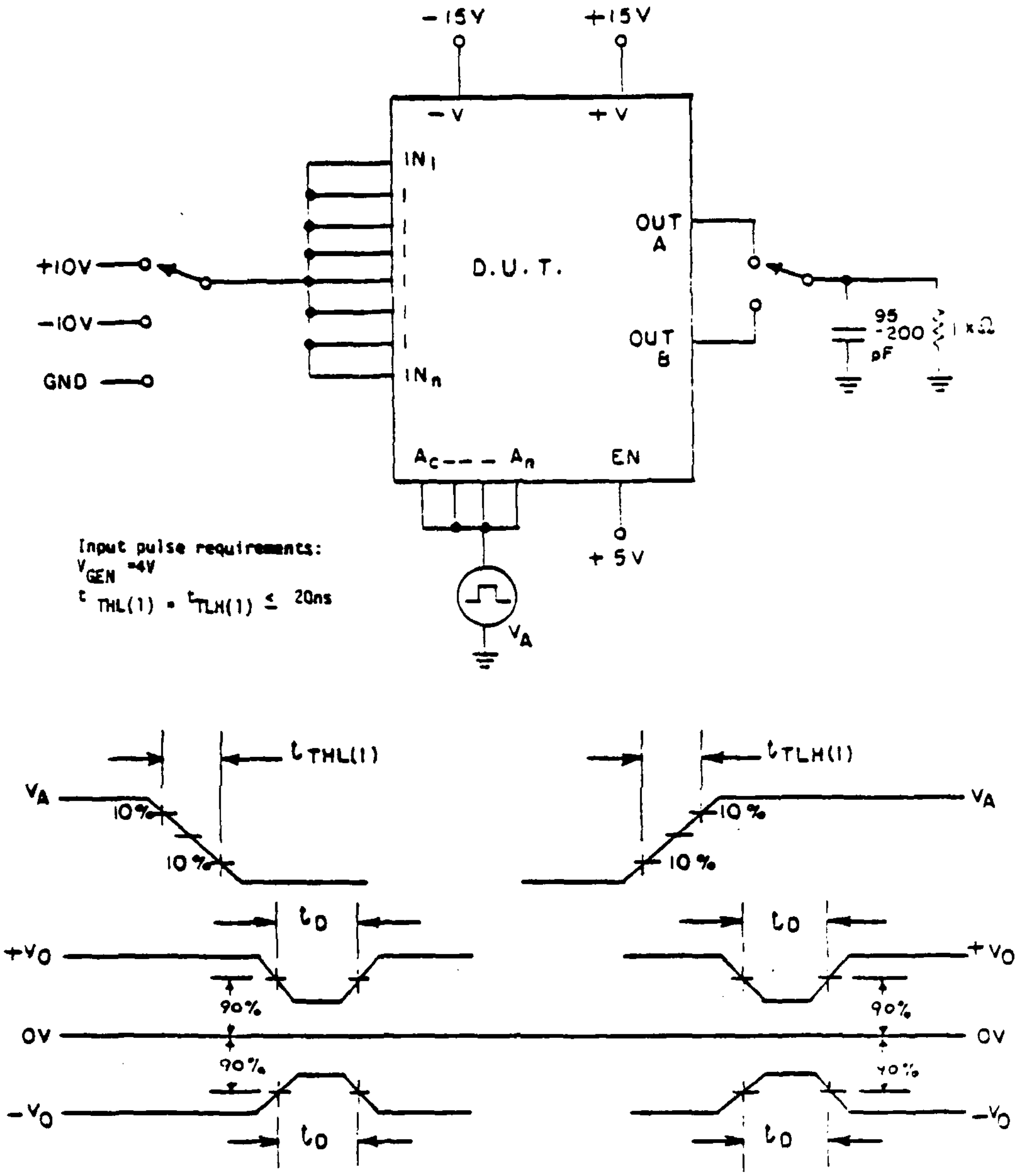


Figure 5.4 Break before make test circuit and waveforms.

This test determines the amount of signal which can leak from an opened switch to the output. For single channel isolation a 1Kohm load is attached to the outputs, and the address lines and the enable are grounded. A one volt peak-to-peak 200KHz sinewave is applied to the inputs by the signal generator (V_{GEN}). The test circuit is shown in figure 5.5. With the enable pin at 0 volts all switches are in the open state. The amount of signal present at the output(s) (V_{OUT}) is measured and V_{ISO} is determined by the equation:

$$V_{ISO}=20\log(V_{GEN}/V_{OUT}).$$

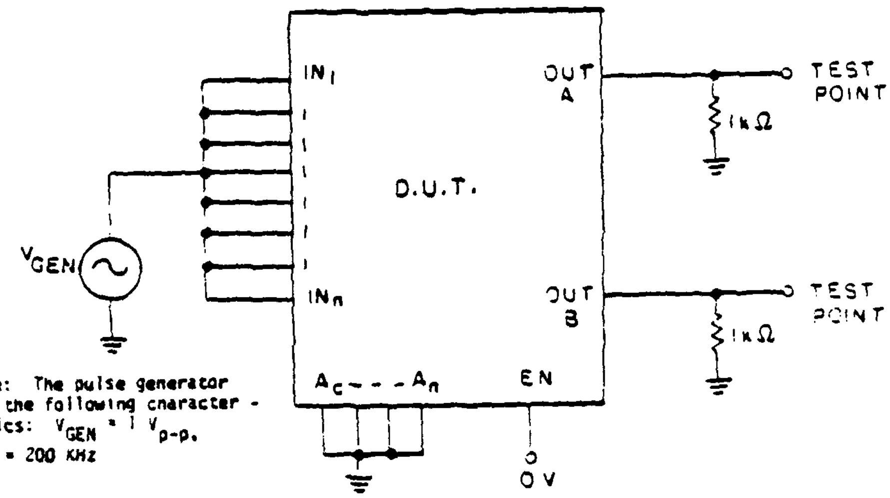
Crosstalk Between Channels (V_{CT})

This test indicates the amount of a signal which passes from an open to a closed switch. The test circuit for crosstalk is shown in figure 5.6. The address lines are connected to ground and a 1Kohm load is placed on the output(s). The enable pin is set to 5 volts; this will activate switch 1 for device types 01,02,05 and 07 and switches 1A,1B for device types 03,04,06 and 08. A 1Kohm load is placed on the active switch inputs. All remaining inputs are connected to the signal generator V_{GEN} (1V p-p 200KHz sinewave). The output peak to peak voltage (V_{OUT}) is measured and V_{CT} is determined by the following equation:

$$V_{CT} = 20\log(V_{GEN}/V_{OUT})$$

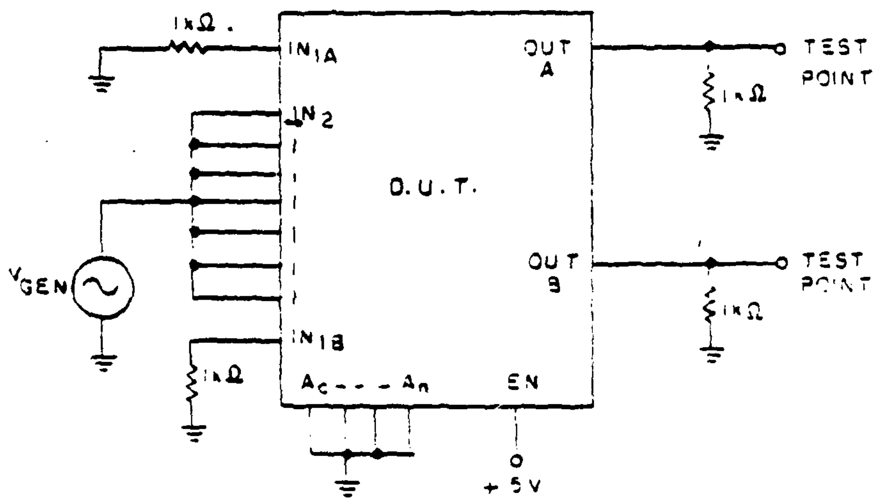
Charge Transfer Error (V_{CTE})

The final test gives an indication of the amount of signal which can be generated at the output(s) due to a signal on the address lines. The test circuit is shown in figure 5.7. In this case the output load(s) consists of a 0.01uf capacitor(s). The input of switch 1 for device types 01,02,05 and 07 (switches 1A and 1B for device types 03,04,06 and 08) are grounded and the remaining inputs are open. The enable pin is set to 5 volts and the address lines are connected to a 0 to 5 volt pulse generator. The output voltage is measured to obtain V_{CTE}.



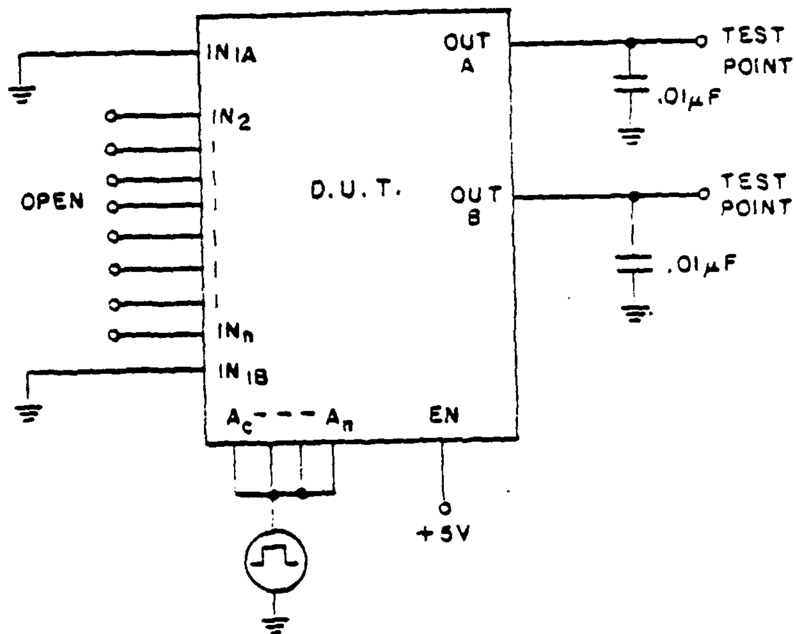
Note: The pulse generator has the following character - istics: $V_{GEN} = 1\ V_{p-p}$, RRR = 200 KHz

Figure 5.5 Single channel isolation test circuit.



Note: The pulse generator has the following characteristics: $V_{GEN} = 1V_{p-p}$; PRR= 200KHz.

Figure 5.6 Crosstalk test circuit.



NOTE: The pulse generator has the following characteristics:
V_{GEN} = 0 - 5V

Figure 5.7 Charge transfer error test circuit.

5.5 Conclusions and Recommendations

The analog multiplexers/demultiolexers from the various manufacturers fully meet the requirements of MIL-M-38510/190C when tested.

5.6 Bibilography

1. Harris Analog Data Book (1982)

2. Siliconix Integrated Circuits Data Book (1985)

3. Intersil Hot Ideas In CMOS Data Book (1983/1984)

5.7 Appendix

Characteristic	Symbol	Conditions 1/ 2/ $V- = -15$ V, $V+ = +15$ V, $V_{EN} = 4.5$ V, GND = 0 V $-55°C < T_A < 125°C$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Positive input clamping voltage	$V_{IC(POS)}$	$T_A = 25°C$, $V+ = V- = 0$ V $I_{IN} = 1$ mA	02,04,05, 06		1.5	V dc
Negative input clamping voltage	$V_{IC(NEG)}$	$T_A = 25°C$, $V+ = V- = 0$ V $I_{IN} = -1$ mA	02,04,05, 06	-1.5		
Input leakage current 3/	I_{IH}	Measure address inputs sequentially, connect all unused address inputs to GND	All	-0.1	+1.0	µA
Input leakage current 3/	I_{IL}	Measure address inputs sequentially connect all unused address inputs to 5 V	All	-1.0	+0.1	
Leakage current into the source terminal of an "OFF" switch	$I_{S(OFF)}$	$V_S = 10$ V, $V_{EN} = 0.8$ V All unused sources = -10 V $T_A = 25°C$	All	-1	1	nA
		$-55°C \leq T_A \leq 125°C$	All	-50	50	
		$V_S = -10$ V, $V_{EN} = 0.8$ V All unused sources to +10 V $T_A = 25°C$	All	-1	1	
		$-55°C \leq T_A \leq 125°C$	All	-50	50	
Leakage current into the drain terminal of an "OFF" switch	$I_{D+(OFF)}$	$V_D = 10$ V, $V_{EN} = 0.8$ V All unused sources to -10 V $T_A = 25°C$	01,02	-20	20	nA
			03,04, 05,06 07,08	-10	10	
		$-55°C \leq T_A \leq 125°C$	01,02,	-500	500	
			03,04 05,07	-250	250	
			06,08	-125	125	
	$I_{D-(OFF)}$	$V_D = -10$ V, $V_{EN} = 0.8$ V All unused sources to +10 V $T_A = 25°C$	01,02	-20	20	
			03,04, 05,06 07,08	-10	10	
		$-55°C \leq T_A \leq 125°C$	01,02,	-500	500	
			03,04 05,07	-250	250	
			05,08	-125	125	

See footnotes at end of table.

Table 5.2 Electrical Parameter Limits

Characteristic	Symbol	Conditions 1/ 2/ $V- = -15$ V, $V+ = +15$ V, $V_{EN} = 4.5$ V, GND = 0 V $-55^\circ C \leq T_A \leq 125^\circ C$ Unless otherwise specified	Device type	Limits		Unit
				Min	Max	
Leakage current from an "ON" driver into the switch (drain)	$I_{D(ON)}$	$V_S = 10$ V, $V_D = 10$ V Connect all unused sources to -10 V $T_A = 25^\circ C$	01,02	-20	20	nA
			03,04, 05,06 07,08	-10	10	
		$-55^\circ C \leq T_A \leq 125^\circ C$	01,02,	-500	500	
			03,04 05,07	-250	250	
			06,08	-125	125	
		$V_S = -10$ V, $V_D = -10$ V Connect all unused sources to 10 V $T_A = 25^\circ C$	01,02	-20	20	
			03,04, 05,06 07,08	-10	10	
		$-55^\circ C \leq T_A \leq 125^\circ C$	01,02,	-500	500	
			03,04 05,07	-250	250	
			06,08	-125	125	
Overvoltage protected, leakage current into the drain terminal of an "OFF" switch	$I_{D(OFF)}$ overvoltage	$V_S = 33$ V, $V_D = 0$ V, $V_{EN} = 0.8$ V	02,04,05, 06	-2.0	2.0	µA
		$V_S = -33$ V, $V_D = 0$ V, $V_{EN} = 0.8$ V	02,04,05, 06	-2.0	2.0	
Positive supply current	I(+)	$V_A = 0$ V, $V_{EN} = 5$ V	01,03		14	mA
			02,04,05, 06		2.0	
			07,08		12	
Negative supply current	I(-)	$V_A = 0$ V, $V_{EN} = 5$ V	01,03	-14		
			02,04,05, 06	-1		
			07,08	-12		
Standby positive supply current	I+SBY	$V_A = 0$ V, $V_{EN} = 0$ V	01,03		3.0	mA
			02,04,05, 06		2.0	
			07,08		3.5	
Standby negative supply current	I-SBY	$V_A = 0$ V, $V_{EN} = 0$ V	01,03	-4.0		
			02,04,05, 06	-1.0		
			07,08	-3.5		

See footnotes at end of table.

Table 5.2 (Cont.) Electrical Parameter Limits

Characteristic	Symbol	Conditions 1/ 2/ $V- = -15$ V, $V+ = +15$ V, $V_{EN} = 4.5$ V, GND = 0 V $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ Unless otherwise specified			Device type	Limits Min	Max	Unit
Capacitance: Address	C_A	$V+ = V- = 0$ V, $T_A = 25^{\circ}C$ f = 1 MHz			All		10	pF
Capacitance: Enable	C_{EN}	$V+ = V- = 0$ V, $T_A = 25^{\circ}C$ f = 1 MHz			All		10	pF
Capacitance: Output switch	C_{OS}	$V+ = V- = 0$ V See table III			01		90	pF
					02		85	
					03,04		50	
					05,07		45	
					06,08		25	
Capacitance: Input switch	C_{IS}	$V+ = V- = 0$ V See table III			All		10	
Switch "ON" resistance	R_{DS1}	$V_S = 10$ V	$I_D = 1$ mA	$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$	01,03		500	Ω
				$T_A = 125^{\circ}C$			700	
			$I_D = 100$ µA	$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$	02,04		1,500	
				$T_A = 125^{\circ}C$			2,000	
				$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$	05,06		1,500	
				$T_A = 125^{\circ}C$			1,300	
			$I_D = 1$ mA	$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$	07,08		400	
				$T_A = 125^{\circ}C$			500	

See footnotes at end of table.

Table 5.2 (Cont.) Electrical Patameter Limits

Characteristic	Symbol	Conditions 1/ 2/ V- = -15 V, V+ = +15 V, V_{EN} = 4.5 V, GND = 0 V -55°C < T_A < 125°C Unless otherwise specified			Device type	Limits Min	Limits Max	Unit
Switch "ON" resistance	R_{DS1}	V_S = -10 V	I_D = -1 mA	T_A = 25°C T_A = -55°C	01,03		600	Ω
				T_A = 125°C			700	
			I_D = -100 µA	T_A = 25°C T_A = -55°C	02,04		1,500	
				T_A = 125°C			2,000	
				T_A = 25°C T_A = -55°C	05,06		1,500	
				T_A = 125°C			1,300	
			I_D = -1 mA	T_A = 25°C T_A = -55°C	07,08		400	
				T_A = 125°C			500	
	R_{DS2}	V+ = 10 V, V- = -10 V V_S = 7.5 V		I_D = 1 mA	01,03,07,08		1,000	
				I_D = 100 µA	02,04		2,400	
					05,06		2,200	
		V+ = 10 V, V- = -10 V V_S = -7.5 V		I_D = -1 mA	01,03,07,08		1,000	
				I_D = -100 µA	02,04		2,400	
					05,06		2,200	
Single channel isolation	V_{ISO}	f = 200 kHz, V_{GEN} = 1 Vp-p See figure 17			All	50		dB
Crosstalk between channels	V_{CT}	f = 200 kHz, V_{GEN} = 1 Vp-p See figure 18			All	50		dB
Charge transfer error	V_{CTE}	V_S = GND, see figure 19			All		10	mV

See footnotes at end of table.

Table 5.2 (Cont.) Electrical Parameter Limits

Characteristic	Symbol	Conditions 1/ 2/ V- = -15 V, V+ = +15 V, V_{EN} = 4.5 V, GND = 0 V -55°C ≤ T_A ≤ 125°C Unless otherwise specified		Device type	Limits		Unit
					Min	Max	
Break-before-make time delay	t_D	See figure 16	T_A = 25°C	All	5		ns
Propagation delay times: Address inputs to I/O channels	$t_{ON(A)}$ $t_{OFF(A)}$	R_L = 1 kΩ C_L = 100 pF See figures 8, 10, 12, and 14	T_A = 25°C T_A = -55°C	All		1,000	ns
			T_A = 125°C			1,500	
Enable to I/O	$t_{ON(EN)}$ $t_{OFF(EN)}$	R_L = 1 kΩ C_L = 100 pF See figures 9, 11, 13, and 15	T_A = 25°C T_A = -55°C	All		1,000	
			T_A = 125°C			1,500	

1/ Current flowing in either direction between any associated input and output terminals of the switch shall be 30 mA maximum.

2/ Input = source; Output = drain.

3/ Input current of one input node.

Table 5.2 (Cont.) Electrical Parameter Limits

SECTION VI

DARLINGTON TRANSISTOR ARRAY (2000 SERIES)

MIL-M-38510/141

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LIST OF FIGURES

LIST OF TABLES

6.1 INTRODUCTION

This section of the report reviews the characterization effort for high voltage, high current NPN Darlington Transistor Arrays. Typical applications for the 2000 series darlington transistor array are driving relays, solenoids, lamps, and other devices which have the requirement to be driven from a high voltage, high current source. The 2000 series darlington transistor array is a multi-sourced device with a high DOD system usage. Table I lists the darlington transistor arrays specified for MIL-M-38510/141.

TABLE 1 TABLE OF DEVICE TYPES SPECIFIED

Device	Generic	Manufacturer	Description
01	2001	Sprague	General Purpose, PMOS, CMOS
02	2002	Sprague	14 - 25V PMOS
03	2003	Sprague	5V, TTL, CMOS
04	2004	Sprague	6 - 15V CMOS, PMOS
05	2005	Sprague	High Output TTL

6.2 DESCRIPTION OF DEVICE TYPES

The 2000 series darlington transistor arrays are comprised of seven bipolar silicon NPN darlington pairs which function as inverters. As shown in Figure 1, the emitter of Q1 is connected into the base of Q2 and the collectors of Q1 and Q2 are connected and brought out of the package for the user. The different applications are addressed by changing the components connected to the base of Q1 such as the 7V zener diode, and 10.5K resistor for the 02 device. Furthermore, output protection is achieved with the diodes connected to the collector pair.

6.3 TEST DEVELOPMENT

A list of the darlington transistor array parameters characterized for the respective device types are listed in Table 2.

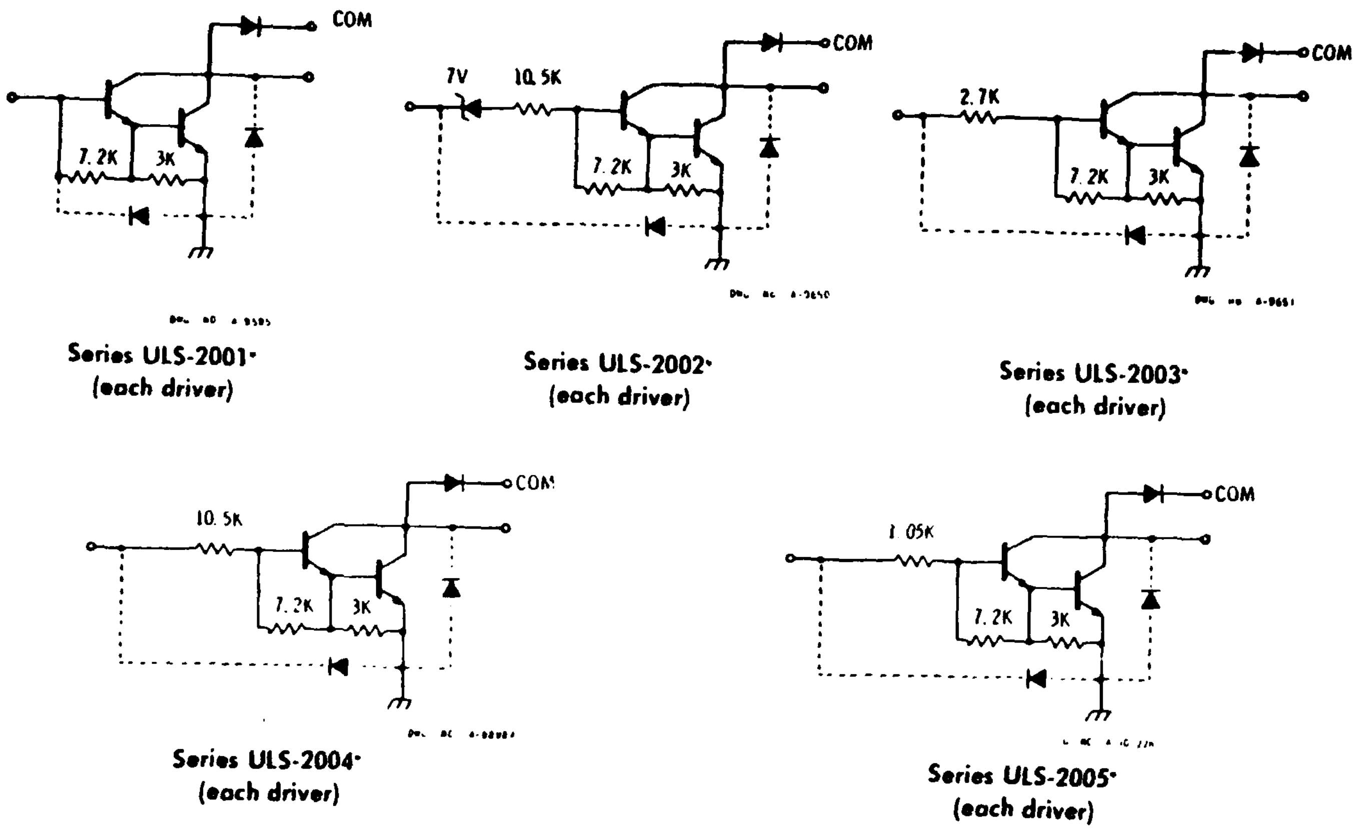


Figure 1 Darlington Transistor Array Schematic (2000 series)

TABLE 2 CHARACTERIZATION PARAMETERS

Item	Symbol	Parameter
1	Icex	Output leakage current
2	V_{CE} (sat)	Collector-emitter saturation voltage
3	I_{IN} (on)	Input current (on)
4	I_{IN} (off)	Input current (off)
5	V_{IN} (on)	Input voltage (on)
6	h_{FE}	DC forward current transfer ratio
7	I_R	Clamp diode leakage current
8	V_F	Clamp diode forward voltage
9	t_{PLH}	Turn-on delay
10	t_{PHL}	Turn-off delay

Test Philosophy:

The approach to testing was to test all dc parameters on the LTX77 Analog Microcircuit Test System and the ac parameters on a bench top test circuit. Bench testing of dc parameters was also performed to prove correlation.

Test Circuits:

The static test circuits are shown in Figure 2 and the dynamic test circuit is shown in Figure 3. All static parameters were measured automatically with the LTX77 Analog Microcircuit Test System. The turn-off delay and turn-on delay parameters were measured on the bench with an oscilloscope due to the limitations of the automatic test equipment utilized.

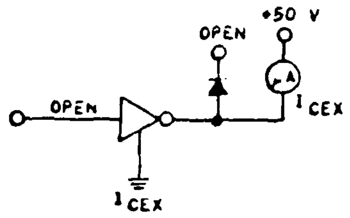


Figure 2a

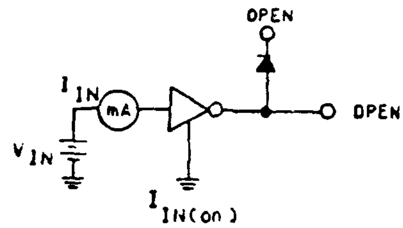


Figure 2b

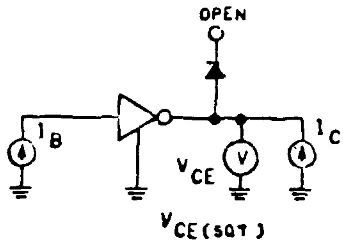


Figure 2c

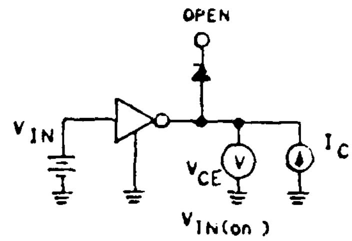


Figure 2d

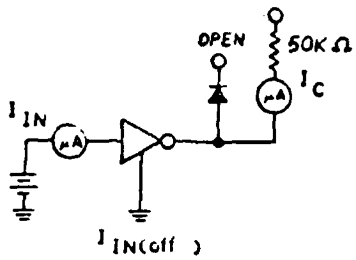


Figure 2e

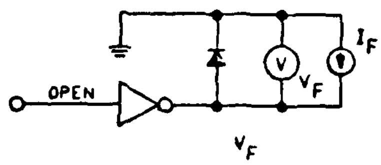


Figure 2f

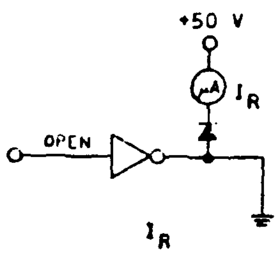
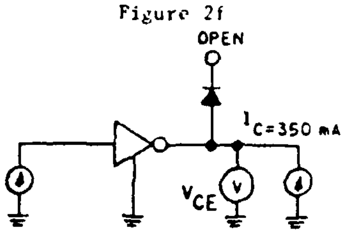


Figure 2g

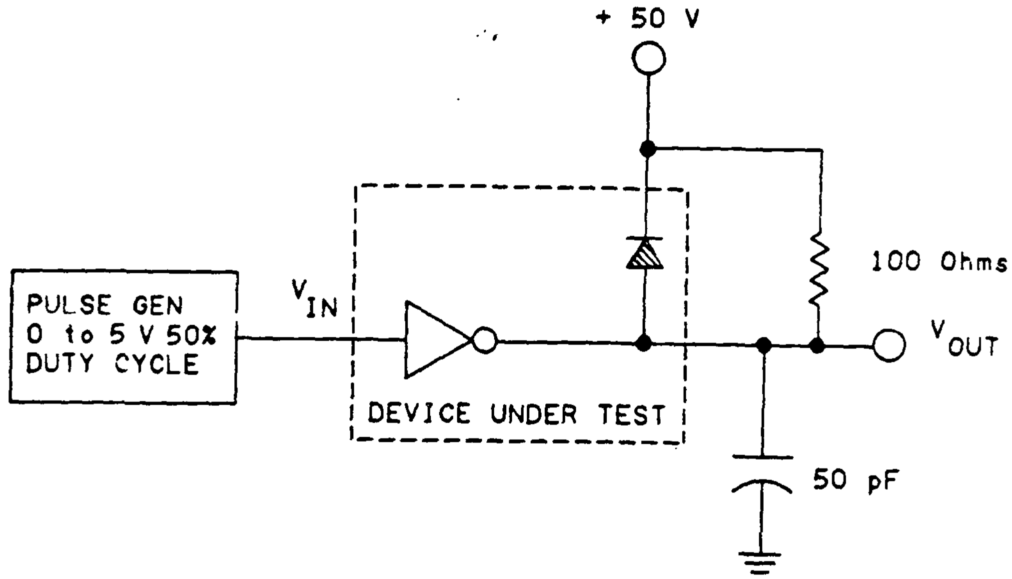


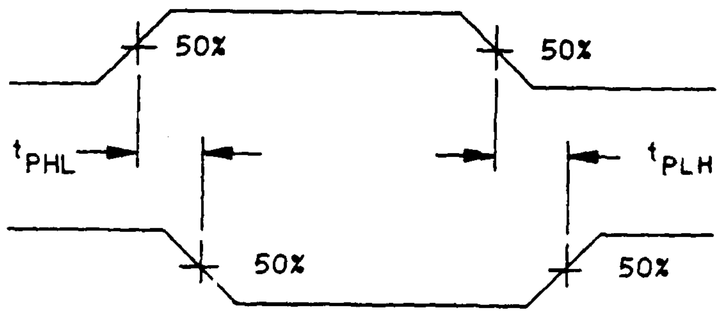
$$h_{FE} = \frac{I_C}{I_B} = \frac{350\ mA}{I_{B\ (MAX)}}$$

Increase current I_b and measure V_{CE}, when $V_{CE} = 2.0$ V record I_b.

Figure 2h

Figure 2 Transistor Array Static Test Circuit





NOTE:
f = 10 KHz
Duty cycle = 50%

Figure 3 Transistor Array Dynamic Test Circuit

6.4 TEST RESULTS AND DISCUSSION

For each parameter measured, the yields were excellent with all data well within the specified limits of the specification.

Output Leakage Current (I_{cex})

The output leakage current measurement was performed by applying 50V to open collectors of the darlington pair and measuring the current across the reverse-biased junction. All the data obtained was well within the specified limit of 10uA (Figure 2a).

Collector-Emitter Saturation Voltage (V_{CE} (sat))

The collector-emitter saturation voltage was measured under three (3) different collector current conditions (I_C = 100mA, 200mA, 350mA). The specified collector current and its respective base current condition were inputted into the darlington pair and the voltage at the output measured to verify that the darlington driver was driven into saturation. All devices passed (Figure 2c).

Input Current On (I_{IN} (on))

The ON input current parameter was measured by applying a specified input voltage and measuring the current into the device. All devices tested were well within the limit of 650uA, minimum and 1350uA maximum (Figure 2b).

Input Current Off (I_{IN} (off))

The OFF input current parameter was measured by applying a known input current to the base of the darlington pair and then measuring the output voltage to assure that the driver was not in the "on" condition (I_c = 500uA). If current

measured on the collector output was greater than 500uA, the device was considered "on" and the part failed this specification. All devices passed this test (Figure 2e).

Input Voltage (on) (V_{IN} (on))

The input ON voltage was measured under three different collector current conditions (I_L = 200mA, 250mA, 300mA). The specified collector current and the respective input voltage were applied to each driver and the output voltage was measured. If the output voltage measured was less than or equal to 2V, the driver was on and the part passed. All device types passed this parameter (Figure 2d).

DC Forward Current Transfer Ratio (h_{FE})

The h_{FE} for the darlington pair was measured by applying 350mA to the open collector and varying the base input until the voltage measured from the collector to emitter equaled 2V. The DC forward current transfer ratio (h_{FE}) was then calculated by the following equation.

$$h_{FE} = I_C/I_B$$

Figure 2h shows the test circuit. All devices passed.

Clamp Diode Leakage Current (I_R)

The clamp diode leakage current was measured by applying 50V to the COM node (pin 9) and then measuring the reverse-bias leakage current resulting from the clamp diode. Evaluation of the data obtained revealed that the nominal value was an order of magnitude less than the specified limit. All devices passed this parameter. (Figure 2g)

Clamp diode forward voltage (V_F)

The clamp diode forward voltage was measured by sourcing 350mA into the collector of the darlington pair. The measured voltage across the diode was the clamp diode forward voltage parameter (Figure 2f). All devices passed this parameter.

Turn ON Delay (t_{PLH}); Turn OFF Delay (t_{PHL})

The turn on and turn off delay times were evaluated using Figure 3. As shown by the waveforms in Figure 3, t_{PHL} and t_{PLH} were measured from the 50% point of the input waveform to the 50% point of the output waveform. All device types passed this parameter and were on the average of 300ns faster than the specified limit for both the t_{PHL} and t_{PLH} parameters.

6.5 CONCLUSION AND RECOMMENDATIONS

The data obtained for this evaluation showed that the darlington transistor arrays met or were much better than the specifications published by the manufacturer. These devices should meet all the requirements needed for a high power drivers in DOD system designs.

6.6 BIBLIOGRAPHY

Integrated Circuit Engineering Bulletin, Sprague Electric Company (1979).

6.7 APPENDIX

Included in the Appendix are examples of the data obtained during the characterization effort. Data presented was compiled on the LTX77 automatic system and presented in its long form over all three temperatures of -55°C, 25°C, and 125°C.

DEVICE 9911 DEVICE TYPE: 2001

TEST 1		
1.0	0.490 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.1	0.498 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.2	0.451 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.3	0.526 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.4	0.473 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.5	0.502 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.6	0.483 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2		
2.0	1.276 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.1	1.269 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.2	1.261 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.3	1.253 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.4	1.245 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.5	1.263 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.6	1.252 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3		
3.0	1.052 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.1	1.048 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.2	1.043 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.3	1.039 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.4	1.034 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.5	1.044 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.6	1.038 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4		
4.0	0.900 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.1	0.897 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.2	0.895 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.3	0.893 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.4	0.890 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.5	0.894 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.6	0.892 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 6		
6.0	0.991 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.1	1.313 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.2	0.780 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.3	1.183 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.4	1.322 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.5	0.965 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.6	1.368 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 10		
10.0	0.702 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.1	0.384 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.2	0.529 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.3	0.559 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.4	0.326 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.5	0.331 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.6	0.532 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11		
11.0	1.462 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.1	1.470 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.2	1.465 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.3	1.456 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.4	1.443 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.5	1.629 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.6	1.452 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C

Table 3 Sample Test Data

TEST 12		
12.0	0.745 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.1	0.805 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.2	0.800 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.3	0.713 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.4	0.645 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.5	0.620 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.6	0.568 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13		
13.0	1.321 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.1	1.310 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.2	1.308 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.3	1.300 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.4	1.294 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.5	1.311 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.6	1.302 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14		
14.0	1.137 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.1	1.130 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.2	1.129 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.3	1.124 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.4	1.121 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.5	1.130 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.6	1.125 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
TEST 15		
15.0	1.019 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.1	1.015 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.2	1.015 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.3	1.012 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.4	1.011 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.5	1.015 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.6	1.013 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 17		
17.0	1.359 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.1	1.563 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.2	1.195 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.3	1.522 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.4	1.520 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.5	1.332 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.6	1.445 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 21		
21.0	0.906 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.1	0.705 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.2	0.871 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.3	0.757 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.4	0.521 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.5	0.532 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.6	0.895 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
TEST 22		
22.0	1.668 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.1	1.660 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.2	1.659 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.3	1.639 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.4	1.632 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.5	1.641 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.6	1.644 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C

TEST 23			
23.0	1.270	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.1	1.186	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.2	1.186	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.3	1.154	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.4	1.092	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.5	1.075	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.6	0.926	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
24.0	1.223	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.1	1.216	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.2	1.203	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.3	1.194	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.4	1.184	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.5	1.196	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.6	1.191	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
25.0	0.949	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.1	0.945	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.2	0.937	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.3	0.932	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.4	0.927	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.5	0.934	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.6	0.930	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST 26			
26.0	0.756	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
26.1	0.753	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
26.2	0.750	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
26.3	0.747	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
26.4	0.744	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
26.5	0.748	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
26.6	0.747	V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 28			
28.0	2.155	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
28.1	1.640	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
28.2	2.010	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
28.3	1.798	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
28.4	1.579	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
28.5	1.930	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
28.6	1.307	UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
TEST 32			
32.0	1.347	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.1	1.046	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.2	0.723	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.3	0.623	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.4	0.832	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.5	0.813	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.6	0.586	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33			
33.0	1.651	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.1	1.612	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.2	1.594	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.3	1.574	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.4	1.562	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.5	1.562	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.6	1.376	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

DEVICE 9912 DEVICE TYPE: 2001

TEST 1			
1.0	0.492	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.1	0.508	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.2	0.467	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.3	0.499	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.4	0.431	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.5	0.487	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.6	0.485	UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2			
2.0	1.284	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.1	1.277	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.2	1.255	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.3	1.249	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.4	1.255	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.5	1.252	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.6	1.252	V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3			
3.0	1.053	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.1	1.049	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.2	1.041	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.3	1.035	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.4	1.031	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.5	1.034	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.6	1.033	V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4			
4.0	0.894	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.1	0.891	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.2	0.886	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.3	0.883	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.4	0.881	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.5	0.882	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.6	0.881	V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 6			
6.0	0.873	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.1	1.088	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.2	1.209	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.3	0.918	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.4	1.270	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.5	1.032	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.6	0.798	UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 10			
10.0	0.978	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.1	0.557	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.2	0.306	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.3	0.524	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.4	0.570	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.5	0.307	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.6	0.261	UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11			
11.0	1.695	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.1	1.678	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.2	1.669	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.3	1.651	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.4	1.640	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.5	1.641	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.6	1.640	V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C

TEST 12		
12.0	0.719 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.1	0.844 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.2	0.702 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.3	0.691 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.4	0.595 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.5	0.606 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.6	0.770 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13		
13.0	1.318 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.1	1.311 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.2	1.304 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.3	1.292 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.4	1.292 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.5	1.291 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.6	1.291 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14		
14.0	1.129 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.1	1.123 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.2	1.118 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.3	1.111 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.4	1.111 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.5	1.111 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.6	1.111 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
TEST 15		
15.0	1.009 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.1	1.006 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.2	1.002 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.3	0.999 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.4	0.998 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.5	0.998 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.6	0.998 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 17		
17.0	1.904 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.1	2.157 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.2	1.159 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.3	1.154 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.4	1.317 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.5	1.355 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.6	1.607 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 21		
21.0	1.130 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.1	0.353 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.2	0.392 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.3	0.905 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.4	0.716 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.5	0.216 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.6	0.400 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
TEST 22		
22.0	1.691 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.1	1.677 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.2	1.675 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.3	1.659 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.4	1.655 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.5	1.655 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.6	1.655 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C

TEST 23			
	23.0	1.500 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.1	1.373 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.2	1.411 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.3	1.266 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.4	1.335 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.5	1.160 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.6	1.173 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
	24.0	1.225 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.1	1.218 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.2	1.201 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.3	1.193 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.4	1.182 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.5	1.193 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.6	1.186 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
	25.0	0.950 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.1	0.[illegible]45 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.2	0.935 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.3	0.930 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.4	0.924 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.5	0.[illegible]29 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.6	0.926 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST 26			
	26.0	0.755 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.752 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.747 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.744 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.741 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.743 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.741 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 28			
	28.0	2.345 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	2.013 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	2.322 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	1.809 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	1.795 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	2.019 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	1.524 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
TEST 32			
	32.0	1.500 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.1	1.056 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.2	0.694 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.3	0.661 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.4	0.990 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.5	0.904 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.6	0.503 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33			
	33.0	1.660 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.1	1.621 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.2	1.606 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.3	1.584 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.4	1.571 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.5	1.571 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.6	1.388 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

DEVICE 1672 DEVICE TYPE: 2002

TEST 1		
1.0	0.640 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.1	0.519 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.2	0.623 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.3	0.615 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.4	0.678 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.5	0.598 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.6	0.583 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2		
2.0	1.434 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.1	1.360 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.2	1.367 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.3	1.374 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.4	1.427 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.5	1.346 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.6	1.382 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3		
3.0	1.146 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.1	1.105 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.2	1.108 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.3	1.112 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.4	1.141 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.5	1.097 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.6	1.116 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4		
4.0	0.955 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.1	0.935 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.2	0.936 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.3	0.938 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.4	0.951 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.5	0.931 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.6	0.940 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 5		
5.0	926.576 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.1	950.326 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.2	921.826 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.3	912.326 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.4	912.326 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.5	939.638 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.6	932.514 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
TEST 6		
6.0	1.455 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.1	1.093 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.2	1.457 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.3	0.982 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.4	0.939 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.5	1.239 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.6	0.807 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 7		
7.0	1.343 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.1	1.297 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.2	1.302 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.3	1.305 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.4	1.337 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.5	1.287 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.6	1.310 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C

TEST 8			
	8.0	1.478 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.1	1.419 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.2	1.425 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.3	1.432 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.4	1.472 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.5	1.408 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.6	1.437 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
TEST 9			
	9.0	1.614 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.1	1.545 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.2	1.550 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.3	1.555 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.4	1.607 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.5	1.531 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.6	1.564 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
TEST 10			
	10.0	1.002 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.1	0.954 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.2	0.813 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.3	0.348 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.4	0.394 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.5	0.775 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.6	0.721 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11			
	11.0	1.844 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.1	1.571 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.2	1.564 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.3	1.558 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.4	1.566 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.5	1.535 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.6	1.539 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
TEST 12			
	12.0	2.750 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.1	2.737 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.2	2.871 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.3	2.891 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.4	2.811 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.5	2.980 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.6	3.096 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13			
	13.0	1.446 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.1	1.397 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.2	1.398 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.3	1.401 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.4	1.428 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.5	1.389 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.6	1.414 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14			
	14.0	1.205 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.1	1.180 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.2	1.180 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.3	1.181 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.4	1.196 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.5	1.175 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.6	1.189 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C

TEST 15			
15.0	1.049	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.1	1.036	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.2	1.036	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.3	1.037	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.4	1.044	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.5	1.034	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.6	1.041	V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 16			
16.0	1013.262	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.1	1013.262	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.2	971.700	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.3	988.325	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.4	997.825	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.5	980.013	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.6	980.013	UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
TEST 17			
17.0	3.537	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.1	3.327	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.2	3.226	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.3	3.358	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.4	2.979	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.5	3.825	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.6	3.459	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 18			
18.0	1.350	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
18.1	1.321	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
18.2	1.322	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
18.3	1.324	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
18.4	1.340	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
18.5	1.315	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
18.6	1.331	V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
TEST 19			
19.0	1.464	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
19.1	1.431	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
19.2	1.432	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
19.3	1.435	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
19.4	1.456	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
19.5	1.425	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
19.6	1.445	V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
TEST 20			
20.0	1.582	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
20.1	1.543	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
20.2	1.543	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
20.3	1.545	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
20.4	1.572	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
20.5	1.535	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
20.6	1.558	V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
TEST 21			
21.0	3.594	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.1	2.993	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.2	3.109	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.3	2.826	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.4	2.487	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.5	2.645	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.6	4.154	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C

TEST 22			
	22.0	1.802 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.1	1.774 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.2	1.770 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.3	1.769 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.4	1.793 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.5	1.747 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.6	1.782 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
TEST 23			
	23.0	1.311 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.1	1.177 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.2	1.184 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.3	1.124 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.4	1.151 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.5	1.203 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.6	1.178 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
	24.0	1.383 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.1	1.313 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.2	1.310 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.3	1.314 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.4	1.360 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.5	1.288 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.6	1.325 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
	25.0	1.041 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.1	1.002 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.2	1.000 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.3	1.001 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.4	1.028 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.5	0.988 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.6	1.008 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST 26			
	26.0	0.807 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.788 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.786 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.787 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.800 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.781 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.790 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 27			
	27.0	768.255 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.1	784.879 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.2	789.629 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.3	774.192 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.4	742.130 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.5	765.879 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.6	787.254 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
TEST 28			
	28.0	2.931 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	2.265 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	2.558 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	2.324 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	2.047 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	2.254 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	1.699 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C

TEST 29			
29.0	1.257	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
29.1	1.213	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
29.2	1.210	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
29.3	1.213	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
29.4	1.242	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
29.5	1.197	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
29.6	1.219	V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
TEST 30			
30.0	1.441	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
30.1	1.385	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
30.2	1.383	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
30.3	1.387	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
30.4	1.423	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
30.5	1.365	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
30.6	1.395	V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
TEST 31			
31.0	1.569	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.1	1.504	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.2	1.500	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.3	1.503	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.4	1.549	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.5	1.480	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.6	1.512	V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
TEST 32			
32.0	1.461	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.1	1.185	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.2	1.435	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.3	1.359	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.4	0.974	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.5	0.951	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.6	1.403	UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33			
33.0	1.840	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.1	1.775	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.2	1.770	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.3	1.760	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.4	1.806	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.5	1.716	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.6	1.749	V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

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TEST 1		
1.0	0.515 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.1	0.569 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.2	0.524 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.3	0.566 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.4	0.512 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.5	0.549 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.6	0.486 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2		
2.0	1.446 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.1	1.367 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.2	1.378 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.3	1.384 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.4	1.444 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.5	1.349 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.6	1.390 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3		
3.0	1.147 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.1	1.103 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.2	1.109 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.3	1.112 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.4	1.145 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.5	1.092 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.6	1.115 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4		
4.0	0.948 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.1	0.927 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.2	0.929 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.3	0.930 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.4	0.946 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.5	0.921 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.6	0.931 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 5		
5.0	924.008 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.1	932.320 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.2	907.383 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.3	902.633 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.4	932.514 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.5	907.577 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.6	894.321 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
TEST 6		
6.0	1.068 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.1	1.346 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.2	0.871 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.3	1.336 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.4	1.253 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.5	1.047 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.6	1.382 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 7		
7.0	1.357 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.1	1.307 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.2	1.313 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.3	1.316 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.4	1.356 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.5	1.295 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C
7.6	1.320 V	VOLT. AT INPUT; V(IN)ON=11.8V; 25 DEG. C

TEST 8			
	8.0	1.496 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.1	1.436 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.2	1.444 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.3	1.447 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.4	1.495 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.5	1.421 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
	8.6	1.454 V	VOLT. AT INPUT; V(IN)ON=12.4V; 25 DEG. C
TEST 9			
	9.0	1.637 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.1	1.563 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.2	1.575 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.3	1.580 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.4	1.636 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.5	1.546 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
	9.6	1.587 V	VOLT. AT INPUT;V(IN)ON=13V; 25 DEG. C
TEST 10			
	10.0	1.326 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.1	0.469 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.2	0.434 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.3	0.917 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.4	0.761 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.5	0.272 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.6	0.424 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11			
	11.0	1.912 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.1	1.824 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.2	1.826 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.3	1.830 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.4	1.891 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.5	1.794 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.6	1.829 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
TEST 12			
	12.0	2.090 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.1	1.945 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.2	1.876 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.3	1.900 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.4	1.868 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.5	2.048 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.6	2.048 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13			
	13.0	1.450 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.1	1.405 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.2	1.405 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.3	1.412 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.4	1.447 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.5	1.403 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.6	1.424 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14			
	14.0	1.212 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.1	1.187 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.2	1.187 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.3	1.190 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.4	1.209 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.5	1.185 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.6	1.197 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C

TEST 15			
	15.0	1.056 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.1	1.044 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.2	1.043 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.3	1.045 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.4	1.054 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.5	1.042 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.6	1.048 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 16			
	16.0	964.575 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.1	988.325 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.2	970.513 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.3	1002.575 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.4	1002.575 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.5	997.825 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.6	950.326 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
TEST 17			
	17.0	2.501 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.1	2.518 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.2	2.093 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.3	2.510 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.4	2.524 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.5	2.470 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.6	2.892 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 18			
	18.0	1.359 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
	18.1	1.331 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
	18.2	1.330 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
	18.3	1.334 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
	18.4	1.357 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
	18.5	1.329 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
	18.6	1.341 V	VOLT. AT INPUT;V(IN)ON=16.8V; -55 DEG. C
TEST 19			
	19.0	1.476 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
	19.1	1.441 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
	19.2	1.439 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
	19.3	1.447 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
	19.4	1.474 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
	19.5	1.438 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
	19.6	1.454 V	VOLT. AT INPUT;V(IN)ON=17.4V; -55 DEG. C
TEST 20			
	20.0	1.593 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
	20.1	1.553 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
	20.2	1.552 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
	20.3	1.558 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
	20.4	1.590 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
	20.5	1.551 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
	20.6	1.571 V	VOLT. AT INPUT;V(IN)ON=18V; -55 DEG. C
TEST 21			
	21.0	3.032 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.1	2.148 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.2	2.028 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.3	2.342 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.4	2.224 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.5	1.716 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.6	2.325 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C

TEST 22			
	22.0	1.873 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.1	1.830 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.2	1.823 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.3	1.833 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.4	1.870 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.5	1.823 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.6	1.847 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
TEST 23			
	23.0	1.256 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.1	1.310 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.2	1.198 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.3	1.350 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.4	1.290 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.5	1.365 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.6	1.350 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
	24.0	1.394 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.1	1.320 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.2	1.317 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.3	1.319 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.4	1.368 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.5	1.292 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.6	1.321 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
	25.0	1.045 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.1	1.002 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.2	1.000 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.3	1.001 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.4	1.029 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.5	0.986 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.6	1.001 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST 26			
	26.0	0.805 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.784 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.782 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.783 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.796 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.775 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.782 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 27			
	27.0	752.817 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.1	732.630 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.2	758.755 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.3	797.941 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.4	769.442 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.5	746.880 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.6	765.879 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
TEST 28			
	28.0	2.634 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	2.742 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	2.242 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	2.620 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	2.119 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	1.975 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	2.180 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C

TEST 29			
	29.0	1.266 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
	29.1	1.219 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
	29.2	1.216 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
	29.3	1.217 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
	29.4	1.249 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
	29.5	1.201 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
	29.6	1.217 V	VOLT. AT INPUT;V(IN)ON=11.8V; 125 DEG. C
TEST 30			
	30.0	1.453 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
	30.1	1.397 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
	30.2	1.395 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
	30.3	1.393 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
	30.4	1.432 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
	30.5	1.374 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
	30.6	1.397 V	VOLT. AT INPUT;V(IN)ON=11.4V; 125 DEG. C
TEST 31			
	31.0	1.586 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.1	1.516 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.2	1.513 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.3	1.514 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.4	1.561 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.5	1.489 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.6	1.517 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
TEST 32			
	32.0	1.888 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.1	1.284 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.2	1.179 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.3	1.336 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.4	1.310 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.5	1.059 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.6	1.053 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33			
	33.0	1.875 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.1	1.812 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.2	1.803 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.3	1.797 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.4	1.844 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.5	1.750 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.6	1.781 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

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TEST 1			
	1.0	0.560 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.1	0.442 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.2	0.490 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.3	0.398 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.4	0.459 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.5	0.430 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.6	0.393 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2			
	2.0	1.196 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.1	1.193 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.2	1.186 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.3	1.174 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.4	1.171 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.5	1.178 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.6	1.173 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3			
	3.0	1.008 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.1	1.007 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.2	1.003 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.3	0.996 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.4	0.994 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.5	0.998 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.6	0.995 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4			
	4.0	0.882 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.1	0.882 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.2	0.880 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.3	0.876 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.4	0.876 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.5	0.877 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.6	0.876 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 5			
	5.0	534.049 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.1	548.298 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.2	544.736 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.3	538.798 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.4	534.049 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.5	534.049 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.6	544.736 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
TEST 6			
	6.0	1.302 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.1	0.808 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.2	0.984 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.3	1.140 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.4	0.835 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.5	1.239 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.6	0.877 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 7			
	7.0	1.050 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.1	1.038 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.2	1.049 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.3	1.043 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.4	1.039 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.5	1.038 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.6	1.028 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C

TEST 8			
	8.0	1.230 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
	8.1	1.212 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
	8.2	1.226 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
	8.3	1.216 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
	8.4	1.212 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
	8.5	1.212 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
	8.6	1.194 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
TEST 9			
	9.0	1.584 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
	9.1	1.557 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
	9.2	1.585 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
	9.3	1.563 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
	9.4	1.555 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
	9.5	1.558 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
	9.6	1.528 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
TEST 10			
	10.0	0.749 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.1	0.760 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.2	0.643 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.3	0.268 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.4	0.323 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.5	0.560 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.6	0.503 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11			
	11.0	1.613 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.1	1.415 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.2	1.401 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.3	1.390 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.4	1.384 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.5	1.379 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.6	1.376 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
TEST 12			
	12.0	3.378 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.1	3.222 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.2	3.181 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.3	3.078 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.4	2.605 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.5	2.524 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.6	2.111 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13			
	13.0	1.245 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.1	1.246 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.2	1.241 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.3	1.230 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.4	1.230 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.5	1.234 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.6	1.230 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14			
	14.0	1.093 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.1	1.093 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.2	1.091 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.3	1.084 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.4	1.084 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.5	1.087 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.6	1.085 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C

TEST 15		
15.0	0.994 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.1	0.994 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.2	0.993 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.3	0.990 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.4	0.990 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.5	0.991 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
15.6	0.990 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 16		
16.0	356.929 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.1	368.804 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.2	362.867 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.3	362.867 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.4	348.617 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.5	348.617 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
16.6	348.617 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
TEST 17		
17.0	3.652 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.1	2.908 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.2	3.585 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.3	3.708 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.4	2.933 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.5	3.531 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.6	2.507 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 18		
18.0	1.161 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
18.1	1.150 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
18.2	1.157 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
18.3	1.155 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
18.4	1.153 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
18.5	1.152 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
18.6	1.152 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
TEST 19		
19.0	1.316 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
19.1	1.301 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
19.2	1.311 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
19.3	1.308 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
19.4	1.304 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
19.5	1.304 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
19.6	1.289 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
TEST 20		
20.0	1.634 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
20.1	1.611 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
20.2	1.626 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
20.3	1.618 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
20.4	1.615 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
20.5	1.617 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
20.6	1.588 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
TEST 21		
21.0	2.645 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.1	2.285 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.2	2.463 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.3	2.068 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.4	1.820 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.5	1.955 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.6	2.283 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C

TEST 22			
	22.0	1.632 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.1	1.453 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.2	1.443 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.3	1.432 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.4	1.428 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.5	1.424 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.6	1.422 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
TEST 23			
	23.0	0.866 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.1	0.844 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.2	0.816 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.3	0.777 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.4	0.719 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.5	0.690 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.6	0.648 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
	24.0	1.146 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.1	1.140 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.2	1.127 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.3	1.116 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.4	1.108 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.5	1.118 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.6	1.111 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
	25.0	0.907 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.1	0.904 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.2	0.896 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.3	0.889 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.4	0.885 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.5	0.890 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.6	0.886 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST 26			
	26.0	0.739 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.738 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.734 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.730 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.729 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.731 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.729 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 27			
	27.0	310.432 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.1	316.369 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.2	310.432 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.3	302.119 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.4	310.432 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.5	324.681 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.6	320.118 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
TEST 28			
	28.0	2.093 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	1.604 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	1.914 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	1.430 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	1.828 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	1.854 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	1.613 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C

TEST 29			
	29.0	0.946 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
	29.1	0.932 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
	29.2	0.949 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
	29.3	0.941 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
	29.4	0.929 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
	29.5	0.928 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
	29.6	0.915 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
TEST 30			
	30.0	1.164 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
	30.1	1.139 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
	30.2	1.162 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
	30.3	1.152 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
	30.4	1.137 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
	30.5	1.133 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
	30.6	1.109 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
TEST 31			
	31.0	1.580 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.1	1.539 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.2	1.580 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.3	1.560 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.4	1.533 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.5	1.531 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
	31.6	1.489 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
TEST 32			
	32.0	1.043 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.1	0.933 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.2	0.807 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.3	0.520 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.4	0.490 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.5	0.723 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.6	0.673 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33			
	33.0	1.599 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.1	1.391 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.2	1.369 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.3	1.356 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.4	1.350 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.5	1.345 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.6	1.342 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

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TEST 1			
	1.0	0.459 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.1	0.395 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.2	0.428 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.3	0.382 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.4	0.383 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.5	0.378 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
	1.6	0.317 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2			
	2.0	1.209 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.1	1.205 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.2	1.194 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.3	1.188 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.4	1.182 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.5	1.188 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
	2.6	1.188 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3			
	3.0	1.015 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.1	1.012 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.2	1.007 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.3	1.003 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.4	0.999 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.5	1.003 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
	3.6	1.003 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4			
	4.0	0.884 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.1	0.883 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.2	0.880 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.3	0.879 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.4	0.876 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.5	0.878 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
	4.6	0.878 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 5			
	5.0	493.675 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.1	509.112 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.2	538.798 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.3	522.174 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.4	538.798 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.5	515.049 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
	5.6	520.986 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
TEST 6			
	6.0	1.055 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.1	1.117 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.2	0.847 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.3	1.216 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.4	0.914 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.5	0.742 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
	6.6	1.098 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 7			
	7.0	1.115 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.1	1.098 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.2	1.132 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.3	1.111 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.4	1.109 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.5	1.098 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C
	7.6	1.082 V	VOLT. AT INPUT; V(IN)ON=5V; 25 DEG. C

TEST 8		
8.0	1.331 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
8.1	1.306 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
8.2	1.362 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
8.3	1.327 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
8.4	1.322 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
8.5	1.308 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
8.6	1.284 V	VOLT. AT INPUT; V(IN)ON=6V; 25 DEG. C
TEST 9		
9.0	1.766 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
9.1	1.719 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
9.2	1.820 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
9.3	1.761 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
9.4	1.751 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
9.5	1.723 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
9.6	1.684 V	VOLT. AT INPUT;V(IN)ON=8V; 25 DEG. C
TEST 10		
10.0	1.178 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.1	0.284 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.2	0.271 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.3	0.723 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.4	0.539 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.5	0.092 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
10.6	0.274 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11		
11.0	1.678 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.1	1.486 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.2	1.457 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.3	1.455 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.4	1.446 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.5	1.446 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
11.6	1.448 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
TEST 12		
12.0	1.968 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.1	1.821 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.2	2.016 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.3	2.031 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.4	1.725 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.5	1.660 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
12.6	1.574 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13		
13.0	1.259 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.1	1.255 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.2	1.248 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.3	1.244 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.4	1.239 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.5	1.245 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
13.6	1.248 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14		
14.0	1.103 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.1	1.101 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.2	1.097 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.3	1.094 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.4	1.091 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.5	1.095 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
14.6	1.097 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C

TEST 15			
	15.0	1.003 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.1	1.001 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.2	0.999 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.3	0.998 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.4	0.996 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.5	0.998 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.6	0.999 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 16			
	16.0	319.931 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.1	319.931 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.2	339.117 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.3	348.617 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.4	356.929 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.5	348.617 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.6	330.805 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
TEST 17			
	17.0	2.223 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.1	2.569 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.2	2.258 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.3	2.519 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.4	2.249 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.5	1.975 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.6	2.107 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 18			
	18.0	1.183 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
	18.1	1.173 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
	18.2	1.180 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
	18.3	1.177 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
	18.4	1.173 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
	18.5	1.174 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
	18.6	1.167 V	VOLT. AT INPUT;V(IN)ON=6V; -55 DEG. C
TEST 19			
	19.0	1.348 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
	19.1	1.330 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
	19.2	1.341 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
	19.3	1.338 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
	19.4	1.334 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
	19.5	1.334 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
	19.6	1.320 V	VOLT. AT INPUT;V(IN)ON=8V; -55 DEG. C
TEST 20			
	20.0	1.685 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
	20.1	1.654 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
	20.2	1.675 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
	20.3	1.669 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
	20.4	1.660 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
	20.5	1.662 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
	20.6	1.639 V	VOLT. AT INPUT;V(IN)ON=12V; -55 DEG. C
TEST 21			
	21.0	2.431 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.1	1.501 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.2	1.395 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.3	1.803 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.4	1.600 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.5	1.029 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.6	1.649 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C

TEST 22			
	22.0	1.515 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.1	1.461 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.2	1.449 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.3	1.441 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.4	1.434 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.5	1.432 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.6	1.434 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
TEST 23			
	23.0	0.685 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.1	0.755 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.2	0.654 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.3	0.674 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.4	0.581 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.5	0.580 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.6	0.510 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
	24.0	1.155 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.1	1.149 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.2	1.134 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.3	1.125 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.4	1.116 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.5	1.125 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.6	1.122 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
	25.0	0.912 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.1	0.909 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.2	0.901 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.3	0.895 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.4	0.890 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.5	0.895 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.6	0.893 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST 26			
	26.0	0.742 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.741 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.736 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.734 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.731 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.733 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.732 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 27			
	27.0	303.307 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.1	310.432 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.2	305.682 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.3	293.807 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.4	292.619 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.5	300.932 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.6	305.682 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
TEST 28			
	28.0	2.155 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	1.799 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	1.950 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	1.540 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	1.790 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	1.901 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	1.570 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C

TEST 29		
29.0	0.957 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
29.1	0.942 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
29.2	0.956 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
29.3	0.950 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
29.4	0.939 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
29.5	0.939 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
29.6	0.926 V	VOLT. AT INPUT;V(IN)ON=5V; 125 DEG. C
TEST 30		
30.0	1.178 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
30.1	1.152 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
30.2	1.173 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
30.3	1.165 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
30.4	1.151 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
30.5	1.148 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
30.6	1.125 V	VOLT. AT INPUT;V(IN)ON=7V; 125 DEG. C
TEST 31		
31.0	1.604 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.1	1.562 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.2	1.595 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.3	1.579 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.4	1.557 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.5	1.555 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
31.6	1.513 V	VOLT. AT INPUT;V(IN)ON=13V; 125 DEG. C
TEST 32		
32.0	0.912 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.1	0.732 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.2	0.757 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.3	0.463 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.4	0.404 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.5	0.561 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
32.6	0.603 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33		
33.0	1.382 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.1	0.835 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.2	1.346 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.3	1.270 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.4	0.864 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.5	1.298 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
33.6	1.047 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

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TEST 1		
1.0	0.039 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.1	0.237 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.2	0.247 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.3	0.063 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.4	0.282 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.5	0.271 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.6	1.198 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2		
2.0	1.307 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.1	1.304 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.2	1.289 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.3	1.281 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.4	1.274 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.5	1.286 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.6	1.279 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3		
3.0	1.066 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.1	1.064 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.2	1.055 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.3	1.051 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.4	1.047 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.5	1.053 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.6	1.049 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4		
4.0	0.902 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.1	0.902 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.2	0.897 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.3	0.895 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.4	0.893 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.5	0.896 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.6	0.894 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 5		
5.0	1629.409 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.1	1662.669 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.2	1648.415 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.3	1691.177 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.4	1673.360 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.5	1681.675 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.6	1636.536 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
TEST 6		
6.0	7.771 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.1	8.957 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.2	7.667 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.3	8.174 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.4	7.861 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.5	6.908 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.6	9.952 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 9		
9.0	1.732 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.1	1.756 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.2	1.682 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.3	1.736 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.4	1.651 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.5	1.730 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.6	1.698 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C

TEST	10		
	10.0	0.654 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.1	0.504 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.2	0.843 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.3	0.717 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.4	0.164 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.5	0.321 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.6	0.723 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST	11		
	11.0	1.699 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.1	1.639 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.2	1.623 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.3	1.603 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.4	1.599 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.5	1.602 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.6	1.588 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
TEST	12		
	12.0	0.027 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.1	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.2	0.025 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.3	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.4	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.5	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.6	0.027 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST	13		
	13.0	1.347 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.0	1.345 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.0	1.334 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.0	1.328 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.0	1.326 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.0	1.340 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.0	1.328 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST	14		
	14.0	1.148 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.1	1.147 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.2	1.141 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.3	1.137 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.4	1.136 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.5	1.144 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.6	1.137 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
TEST	15		
	15.0	1.025 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.1	1.024 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.2	1.021 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.3	1.019 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.4	1.018 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.5	1.022 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.6	1.018 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST	16		
	16.0	1420.208 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.1	1468.910 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.2	1477.225 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.3	1521.176 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.4	1490.292 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.5	1521.314 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.6	1458.219 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C

TEST 17			
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
17.0	39.746	UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 20			
20.0	1.715	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
20.1	1.728	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
20.2	1.687	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
20.3	1.696	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
20.4	1.648	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
20.5	1.708	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
20.6	1.677	V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
TEST 21			
21.0	3.658	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.1	2.528	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.2	2.237	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.3	2.344	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.4	2.561	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.5	3.002	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
21.6	4.985	UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
TEST 22			
22.0	1.630	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.1	1.605	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.2	1.596	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.3	1.421	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.4	1.425	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.5	1.41[illegible]	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
22.6	1.408	V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
TEST 23			
23.0	0.024	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.1	0.025	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.2	0.025	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.3	0.022	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.4	0.023	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.5	0.025	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
23.6	0.025	UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
24.0	1.276	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.1	1.268	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.2	1.253	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.3	1.244	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.4	1.233	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.5	1.247	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
24.6	1.241	V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
25.0	0.981	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.1	0.977	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.2	0.968	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.3	0.962	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.4	0.957	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.5	0.964	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
25.6	0.961	V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C

TEST 26			
	26.0	0.782 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.779 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.775 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.773 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.770 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.773 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.771 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST 27			
	27.0	1681.675 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.1	1711.509 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.2	1692.503 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.3	1735.404 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.4	1712.835 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.5	1754.410 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.6	1703.332 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
TEST 28			
	28.0	3.995 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	4.108 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	4.471 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	3.595 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	4.122 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	4.187 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	3.410 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
TEST 31			
	31.0	1.657 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.1	1.685 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.2	1.618 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.3	1.662 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.4	1.579 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.5	1.651 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.6	1.610 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
TEST 32			
	32.0	1.430 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.1	0.925 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.2	0.569 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.3	0.721 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.4	0.904 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.5	0.667 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.6	0.537 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST 33			
	33.0	1.619 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.1	1.578 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.2	1.562 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.3	1.540 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.4	1.522 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.5	1.530 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.6	1.520 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

DEVICE 2295 DEVICE TYPE: 2005

TEST 1		
1.0	0.039 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.1	0.215 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.2	0.219 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.3	0.059 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.4	0.236 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.5	0.221 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
1.6	1.270 UA	OUT. LEAKAGE CURRENT [I(CEX)];25 DEG. C
TEST 2		
2.0	1.328 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.1	1.322 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.2	1.309 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.3	1.300 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.4	1.294 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.5	1.305 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
2.6	1.296 V	V(CE)SAT;I(C)=350MA;I(B)=500UA;25 DEG. C
TEST 3		
3.0	1.080 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.1	1.077 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.2	1.069 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.3	1.064 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.4	1.060 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.5	1.067 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
3.6	1.062 V	V(CE)SAT;I(C)=200MA;I(B)=350UA;25 DEG. C
TEST 4		
4.0	0.912 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.1	0.911 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.2	0.907 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.3	0.904 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.4	0.903 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.5	0.906 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
4.6	0.903 V	V(CE)SAT;I(C)=100MA;I(B)=250UA;25 DEG. C
TEST 5		
5.0	1610.403 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.1	1691.177 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.2	1662.669 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.3	1724.713 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.4	1703.194 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.5	1718.774 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
5.6	1683.000 UA	INPUT CURRENT WITH DEVICE ON; 25 DEG. C
TEST 6		
6.0	2.467 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.1	2.283 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.2	2.829 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.3	2.269 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.4	2.696 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.5	2.942 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
6.6	2.468 UA	INPUT CURRENT WITH DEVICE OFF; 25 DEG. C
TEST 9		
9.0	1.722 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.1	1.745 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.2	1.691 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.3	1.728 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.4	1.667 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.5	1.745 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C
9.6	1.706 V	VOLT. AT INPUT;V(IN)ON=2.4V; 25 DEG. C

TEST 10			
	10.0	1.151 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.1	0.813 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.2	0.303 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.3	0.385 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.4	0.701 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.5	0.641 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
	10.6	0.215 UA	DIODE LEAKAGE CURRENT;I(R); 25 DEG. C
TEST 11			
	11.0	1.652 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.1	1.618 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.2	1.605 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.3	1.583 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.4	1.574 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.5	1.577 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
	11.6	1.567 V	DIODE FORWARD VOLTAGE;V(F); 25 DEG. C
TEST 12			
	12.0	0.024 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.1	0.024 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.2	0.024 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.3	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.4	0.024 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.5	0.023 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
	12.6	0.025 UA	OUT. LEAKAGE CURRENT [I(CEX)];-55 DEG. C
TEST 13			
	13.0	1.365 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.1	1.364 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.2	1.353 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.3	1.345 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.4	1.342 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.5	1.351 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
	13.6	1.343 V	V(CE)SAT;I(C)=350MA;I(B)=850UA;-55 DEG. C
TEST 14			
	14.0	1.156 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.1	1.154 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.2	1.148 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.3	1.143 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.4	1.142 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.5	1.147 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
	14.6	1.143 V	V(CE)SAT;I(C)=200MA;I(B)=550UA;-55 DEG. C
TEST 15			
	15.0	1.027 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.1	1.027 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.2	1.023 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.3	1.020 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.4	1.020 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.5	1.022 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
	15.6	1.020 V	V(CE)SAT;I(C)=100MA;I(B)=350UA;-55 DEG. C
TEST 16			
	16.0	1397.639 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.1	1477.225 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.2	1473.662 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.3	1528.441 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.4	1506.922 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.5	1515.237 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C
	16.6	1473.662 UA	INPUT CURRENT WITH DEVICE ON; -55 DEG. C

TEST 17			
	17.0	27.252 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.1	25.362 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.2	21.985 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.3	18.950 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.4	17.074 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.5	13.486 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
	17.6	10.541 UA	INPUT CURRENT WITH DEVICE OFF; -55 DEG. C
TEST 20			
	20.0	1.727 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
	20.1	1.731 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
	20.2	1.694 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
	20.3	1.704 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
	20.4	1.659 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
	20.5	1.719 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
	20.6	1.683 V	VOLT. AT INPUT;V(IN)ON=3.0V; -55 DEG. C
TEST 21			
	21.0	3.735 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.1	3.146 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.2	3.036 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.3	2.740 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.4	2.785 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.5	3.586 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
	21.6	9.427 UA	DIODE LEAKAGE CURRENT;I(R); -55 DEG. C
TEST 22			
	22.0	1.632 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.1	1.608 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.2	1.597 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.3	1.579 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.4	1.573 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.5	1.577 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
	22.6	1.571 V	DIODE FORWARD VOLTAGE;V(F); -55 DEG. C
TEST 23			
	23.0	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.1	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.2	0.025 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.3	0.025 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.4	0.024 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.5	0.026 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
	23.6	0.025 UA	OUT. LEAKAGE CURRENT [I(CEX)];125 DEG. C
TEST 24			
	24.0	1.309 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.1	1.300 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.2	1.284 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.3	1.273 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.4	1.264 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.5	1.277 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
	24.6	1.268 V	V(CE)SAT;I(C)=350MA;I(B)=500;UA;125 DEG. C
TEST 25			
	25.0	1.000 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.1	0.995 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.2	0.986 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.3	0.980 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.4	0.974 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C

	25.5	0.981 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
	25.6	0.976 V	V(CE)SAT;I(C)=200MA;I(B)=350;UA;125 DEG. C
TEST	26		
	26.0	0.792 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.1	0.790 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.2	0.785 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.3	0.782 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.4	0.779 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.5	0.783 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
	26.6	0.780 V	V(CE)SAT;I(C)=100MA;I(B)=250;UA;125 DEG. C
TEST	27		
	27.0	1667.420 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.1	1729.465 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.2	1711.647 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.3	1760.349 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.4	1729.465 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.5	1741.343 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
	27.6	1703.194 UA	INPUT CURRENT WITH DEVICE ON; 125 DEG. C
TEST	28		
	28.0	3.210 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.1	3.547 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.2	3.859 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.3	3.469 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.4	3.687 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.5	3.626 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
	28.6	3.467 UA	INPUT CURRENT WITH DEVICE OFF; 125 DEG. C
TEST	31		
	31.0	1.663 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.1	1.691 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.2	1.623 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.3	1.660 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.4	1.582 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.5	1.656 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
	31.6	1.607 V	VOLT. AT INPUT;V(IN)ON=2.4V; 125 DEG. C
TEST	32		
	32.0	1.259 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.1	0.610 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.2	0.580 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.3	0.762 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.4	0.770 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.5	0.394 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
	32.6	0.479 UA	DIODE LEAKAGE CURRENT;I(R); 125 DEG. C
TEST	33		
	33.0	1.611 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.1	1.574 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.2	1.553 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.3	1.531 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.4	1.513 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.5	1.521 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C
	33.6	1.512 V	DIODE FORWARD VOLTAGE;V(F); 125 DEG. C

SECTION VII

REGULATING PULSE WIDTH MODULATORS

MIL-M-38510/126A

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7.1 INTRODUCTION

This section reviews the characterization effort for Regulating Pulse Width Modulators (PWM) which are replacing conventional shunt regulators in many power supply applications. Shunt regulator type power supplies operate in a continuous mode and dissipate large amounts of power when the difference between input and output voltage is large. The PWM type power supply, however, switches an output transistor to regulate duty cycle. The transistor is, therefore, either saturated or cutoff which allows high efficiency operation. This high efficiency makes pulse width modulator devices good candidates for inclusion into the MIL-M-38510 general specification system. The device types specified in MIL-M-38510/126 are listed in Table 7.1. The list of manufacturers represent those which were evaluated.

TABLE 7.1 DEVICE TYPE SPECIFICATION

Device	General	Manufacturer	Description
01	1524	LT, SG, U	General Purpose
02	1525	SG, U	Totem-pole 200mA Output NOR Logic
03	1526	LT, M, SG, U	TTL/CMOS Logic Parts
04	1527	LT	Same as 1525 OR Logic Output

LT - Linear Technology

M - Motorola

SG - Silicon General

U - Unitrode

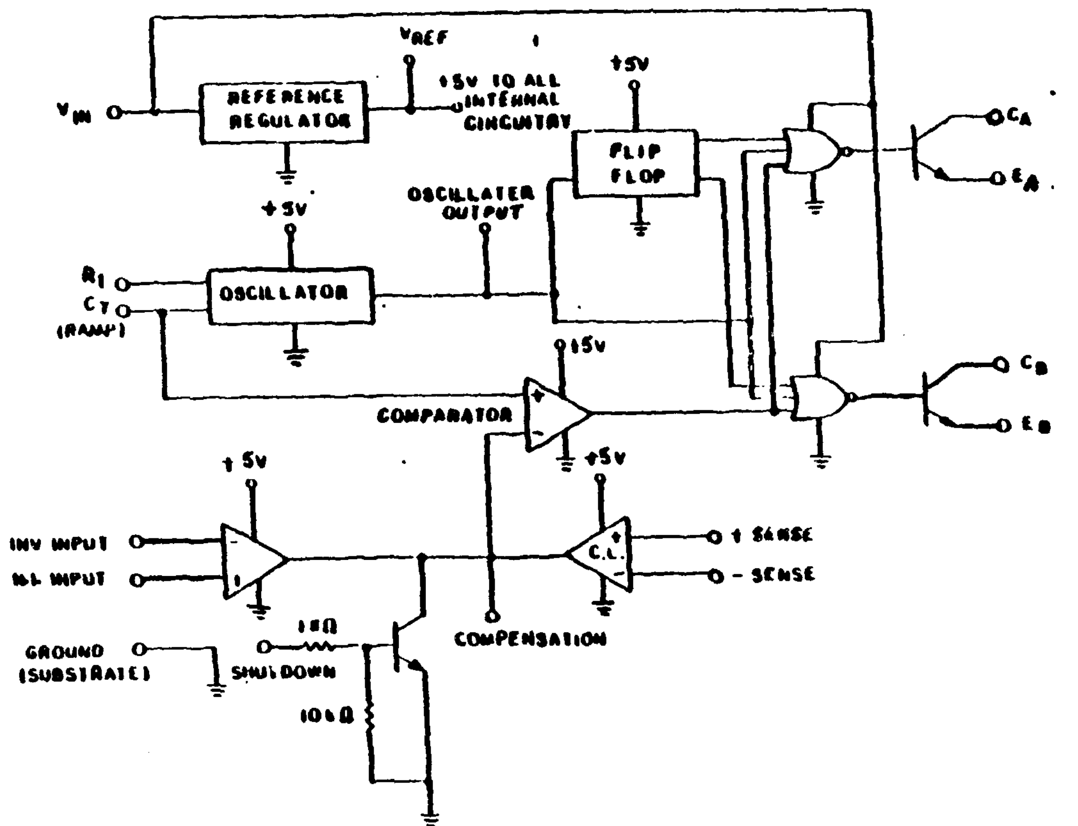
7.2 DESCRIPTION OF DEVICE TYPES

A pulse width modulator requires the following four basic elements for operation: voltage reference, error amplifier, oscillator and differential voltage comparator.

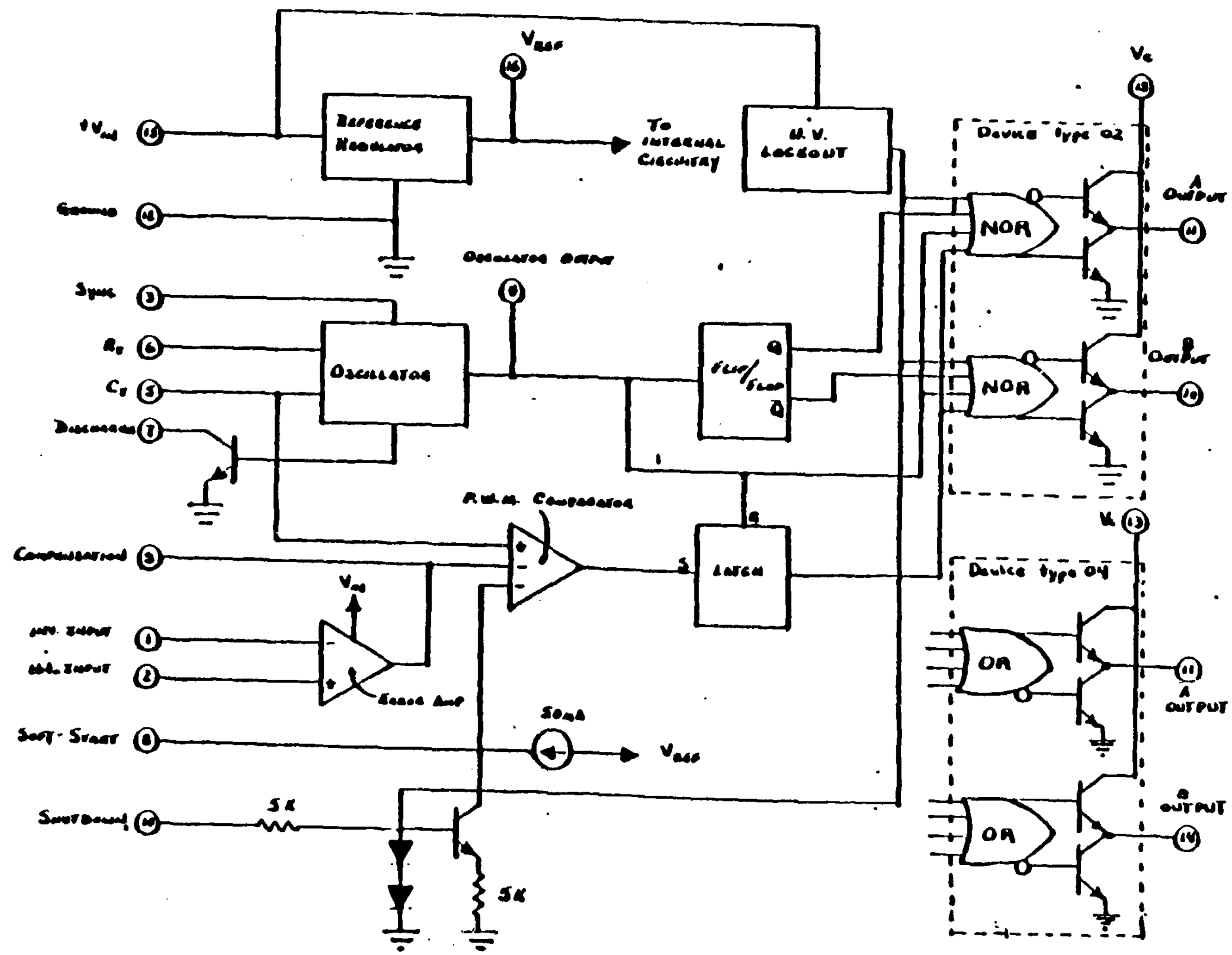
The voltage reference provides the stable reference source for the internal circuitry. A transconductance amplifier is used in the error amplifier design to provide output impedances greater than two mega ohms. The oscillator whose frequency is obtained using an external resistor (R_T) and capacitor (C_T)produces two waveforms. The first waveform is a logic clock used for internal synchronization; the second is a sawtooth waveform which the voltage comparator combines with the error amplifier output and an external compensation pin to vary the duty cycle of the output transistors.

Figure 7.1 contains the block diagrams of device types 01 through 04. By examining the diagrams apparent differences can easily be seen. Device type 01 is the 1524 and is the oldest of the pulse width modulator designs. It includes the four previously discussed elements as well as a current limiter, shutdown circuit and output stage. The current limiter decreases output pulse width when the input threshold is greater than 200mv. The shutdown circuit removes the drive signal from the comparator to deactivate the output. The output consists of two NPN transistors with open collectors and emitters, which allow switching of either PNP or NPN transistors.

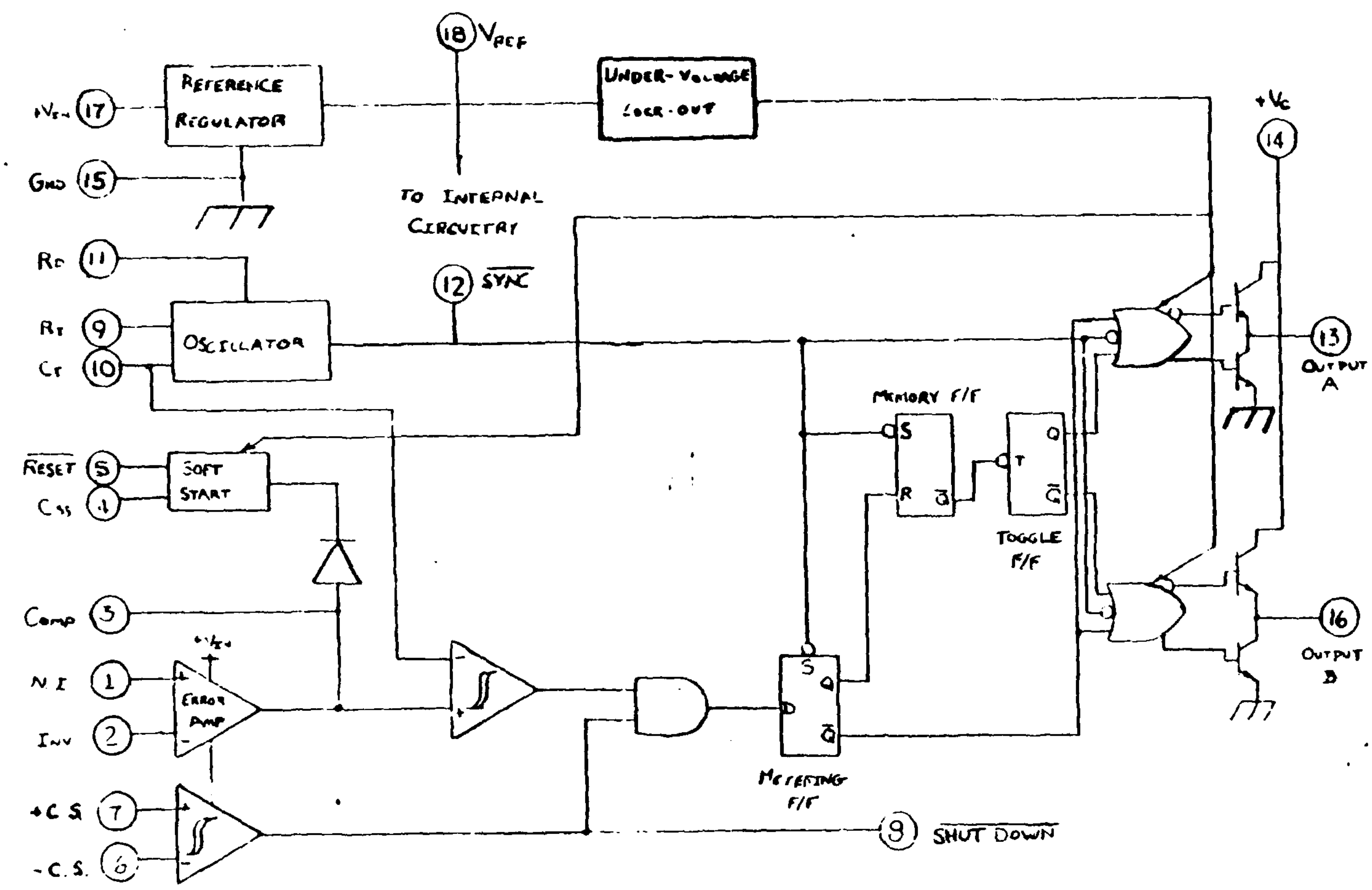
The 1525 and 1527 (Device types 02 and 04) are identical with the exception that the 1525 contains a logical NOR gate in the output stage whereas the 1527 contains a logical OR gate. The following discussion is relevant to both of the devices. Since both devices are based on the 1524, only their differences will be described. The dead time can now be controlled in these later designs by using a small resistor (RD less than 100 ohm) connected between the discharge pin and the C_T pin. By using a capacitor on pin 8, the soft start circuitry gradually increases the duty cycle of the output transistor as the supply voltage is increased over 8 volts. As the capacitor charges to its full potential, the error amplifier takes



Device Type 01
Figure 7-1 Block Diagram



Device Type 02, 04
Figure 7-1 (cont.) Block Diagram



Device Type 03
Figure 7-1 (cont.) Block Diagram

control of the comparator, allowing a steady and even powering of the device. The outputstage has been redesigned into a totem-pole configuration which has a low impedance in both the "on" and "off" state. Logic in the 1525 yields a high output pulse during a transistor on state while the 1527 gives a high output pulse during the transistor "off" state. The final element added was the undervoltage lockout which is activated if the supply voltage is less than 8 volts.

The 1526 is similar to the 1525 in that it contains an error amplifier, comparator, oscillator, reference, undervoltage lockage, soft start, and shutdown. The improvements include the addition of three digital ports (RESET, SYNC and SHUTDOWN) capable of driving TTL and 5V CMOS logic directly. The digital ports are normally at a high state and are activated by driving them low. Pulling RESET low will discharge the soft start capacitor. Releasing RESET allows the device to slowly turn on. The SHUTDOWN pin being pulled LOW will inhibit all output pulses. The final port, SYNC, is used to control the frequency via an external source.

The error amplifier common mode range in the 1524 is 1.8V to 3.4V which was found to be inadequate due to the fact that the range did not cover the reference voltage (5.1V) and ground. The 1525/1527 improved on this by having a range of 1.5V to 5.2V, however, ground was still not in the common mode range. The error amplifier of the 1526 corrects all of the above problems by having a range of 0V to 5.2V.

7.3 TEST DEVELOPMENT

A list of parameters used to characterize the pulse width modulators are contained in Table 7.2. The table contains the parameters which are common to all four device types. The parameters which are unique to various PWM's are listed in Table 7.3.

TABLE 7.2 TEST PARAMETERS

Symbol	Parameter	Element
V_{IO}, I_{IO}	Input Offset Voltage and Current	Error Amplifier
I_{IB}	Bias Current	
CMR	Common Mode Rejection	
A_{VS}	Voltage Gain	
SVRR	Supply Voltage Rejection Ratio	
G_{BW}	Unity Gain Bandwidth	
V_{REF}	Output Voltage	Reference
V_{RLINE}, V_{RLOAD}	Line and Load Regulation	
$\Delta V_{IN}/\Delta V_{REF}$	Ripple Rejection	
I_{OS}	Short Circuit Current	
N_O	Noise Voltage	
fosc	Initial Frequency	Oscillator
fosc(min), (max)	Minimum, Maximum Frequency	
$\Delta fosc/\Delta V_{IN}$	Voltage Stability	
tpw	Clock Pulse Width	
V_{RAMP}	Ramp Voltage	
T_R, T_F	Rise and Fall Time	Output
I_C	Collector Current	
V_{OH}, V_{OL}	Output High, Output Low	
ton/tosc	Minimum and Maximum Duty Cycle	Comparator
I_{in}	Power Supply Current	

TABLE 7.3 ADDITIONAL TEST PARAMETERS

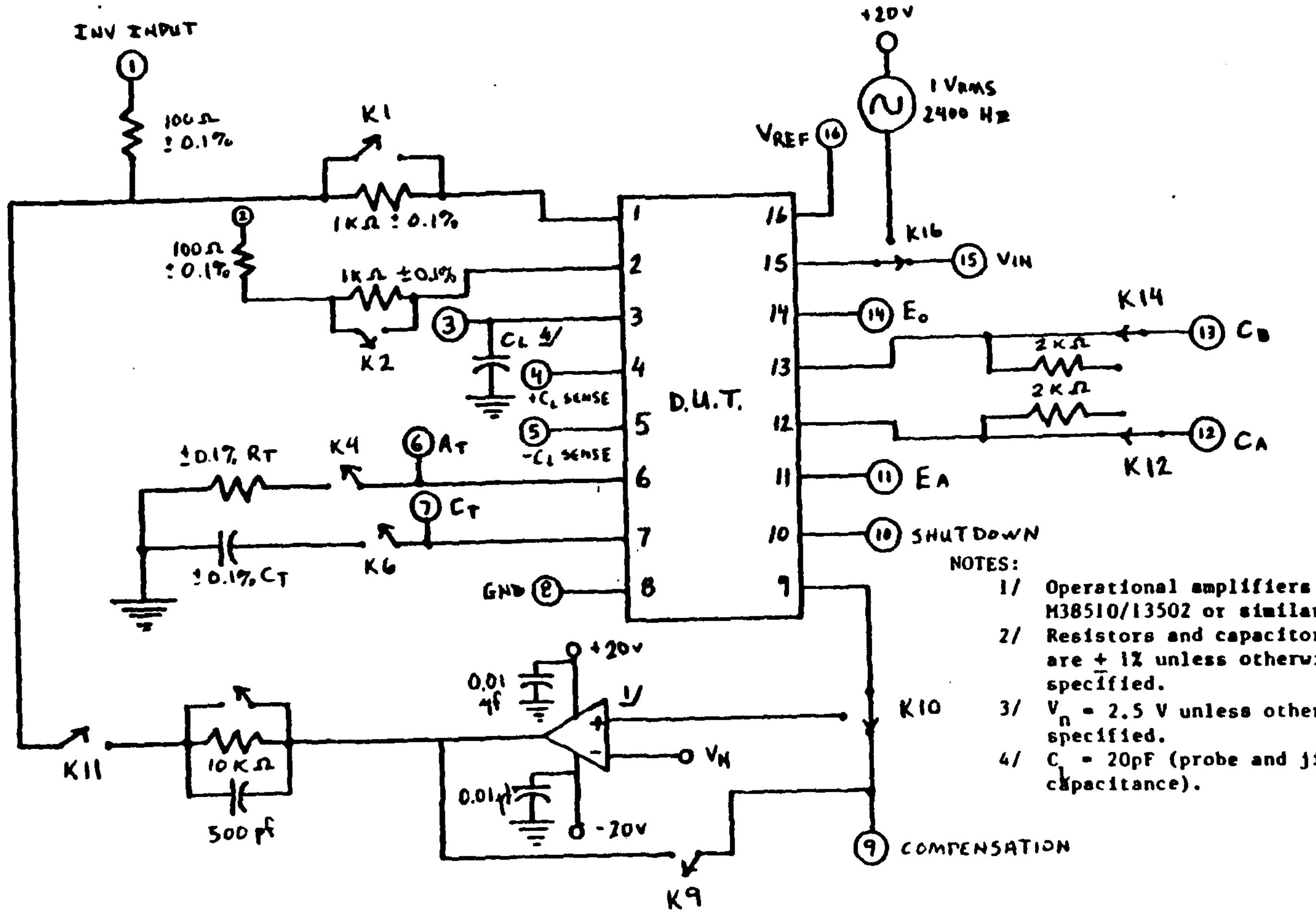
Device Type	Symbol	Test Parameters
01	V_{SEN}	Current Limit Sense Voltage
	V_{SD}	Shutdown Voltage
02, 04	I_{SS}, V_{SS}	Soft Start Current, Voltage
	I_{SD}, V_{SD}	Shutdown Current, Voltage
03	V_S	Current Limit Comp., Sense Voltage
	I_{IBS}	Current Limit Comp., Bias Current
	I_{IL}, I_{IH}	Input Current, Digital Ports
	V_{OLP} V_{OHP}	Output Voltage, Digital Ports
	V_R	Under Voltage Lockout
	I_{CS}	Capacitor Charging Current
	V_{EC}	Error Clamp Voltage

The majority of the testing for these parameters was performed using bench top test circuits (shown in Figure 7.2) and equipment, with a limited amount of Automatic Test Equipment being utilized to evaluate the 1524.

7.4 TEST RESULTS AND DISCUSSION

Error Amplifier:

In order to perform proper testing, a nulling amplifier must be used, such as the OP07 which was used in our case. The nulling amp suppresses the natural oscillation tendencies of the error amplifier (E.A.), and also controls the output.



NOTES:

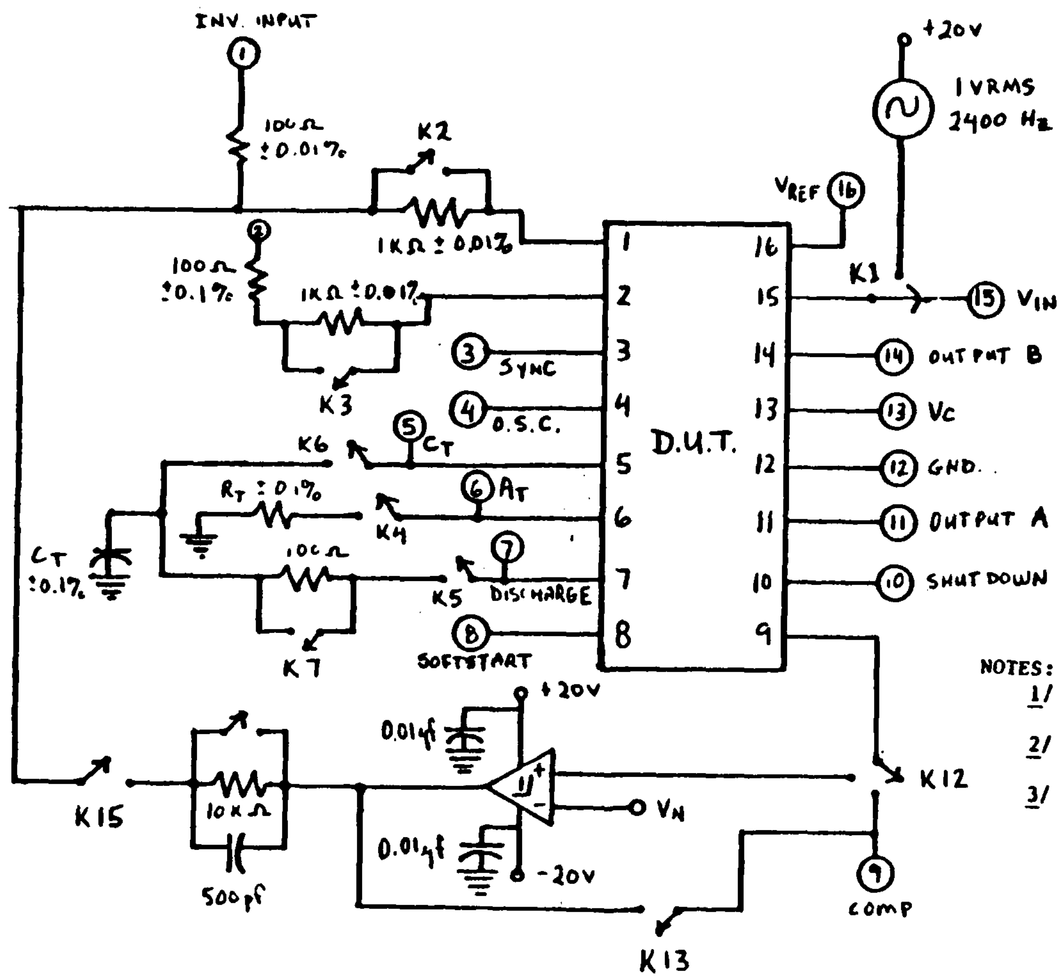
1/ Operational amplifiers are M38510/13502 or similar.

2/ Resistors and capacitors are ± 1% unless otherwise specified.

3/ V_n = 2.5 V unless otherwise specified.

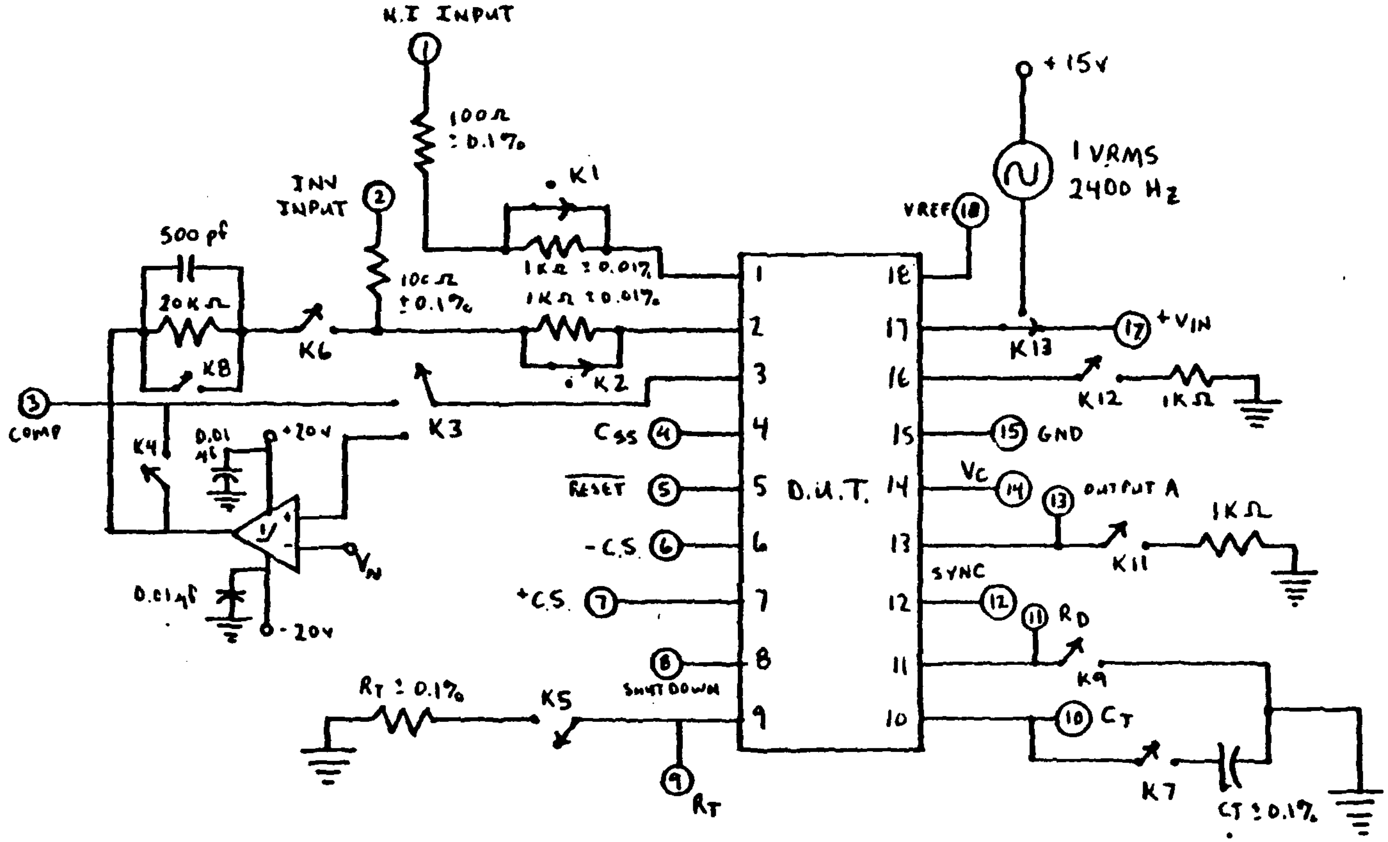
4/ C_L = 20pF (probe and jig capacitance).

Device Type 01
Figure 7-2 Test Circuit



NOTES:
1/ Operational amplifiers are M38510/13502 or similar.
2/ Resistors and capacitors are ± 1% unless otherwise specified.
3/ $\overline{V}_N$ = 2.5 V unless otherwise specified.

Device Type 02, 04
Figure 7-2 (cont.) Test Circuit



NOTES:

1/ Operational amplifiers are M38510/13502 or similar.

2/ Resistors and capacitors are ± 1% unless otherwise specified.

3/ $\overline{V}_N$ = 2.5 V unless otherwise specified.

Device Type 03

Figure 7-2 (cont.) Test Circuit

The two input voltages are set to 2.5 volts (the center of the error amp common mode range) and V_N is equal to OV for the following tests: Input Offset Voltage V_{IO}. Input Bias Current I_{IB}, and Input Offset Current I_{IO}, The test circuit is shown in Figure 7.3. The offset voltage is determined by the following equation V_{IO} = V_O/Gain, (V_O is measured with relays K1 and K2 closed). The input bias currents are determined by the following method: For I_{IB+}, close the K1 relay, open the K2 relay and measure V_{01} at the output of the error amplifier; $I_{IB+} = (V_O - V_{01})/(\text{Gain} \times 1000)$. For I_{IB-}, open the K1 relay, close the K2 relay and measure V_{02} at the output. $I_{IB-} = (V_0 - V_{02})/(\text{Gain} \times 1000)$. The offset current I_{IO} is determined by taking the difference between the plus and minus bias currents.

For the common mode rejection (CMR), the V_N is set to 0 volts and the input voltage to the error amplifier is varied over the common mode range (V_{cm}); this is different for each device type.

$$CMR = 20 \log (\Delta V_{cm}/\Delta V_O) \times \text{gain}$$

For both the gain (A_{VS}) and supply voltage rejection (SVRR) tests, V_{IN} is set to 2.5 volts. The voltage gain A_{VS} measurement is performed by varying the negative input of the nulling Amp (V_N) over the common mode range of the EA, and measuring the change in V_O.

$$A_{VS} = 10\log ((\Delta V_N/\Delta V_O)^* \text{ gain})$$

The SVRR is determined by varying the supply voltage to the chip and measuring the change in V_O.

$$SVRR = 20 \log ((\Delta V_{CC}/\Delta V_O)^* \text{ gain})$$

Unity Gain Bandwidth (G_{BW}) must be determined using a separate test circuit as shown in Figure 7.4. The G_{BW} is measured by increasing the frequency of e_i, starting at 100KHz, until the magnitude of $e_o = e_i$. The frequency at which this

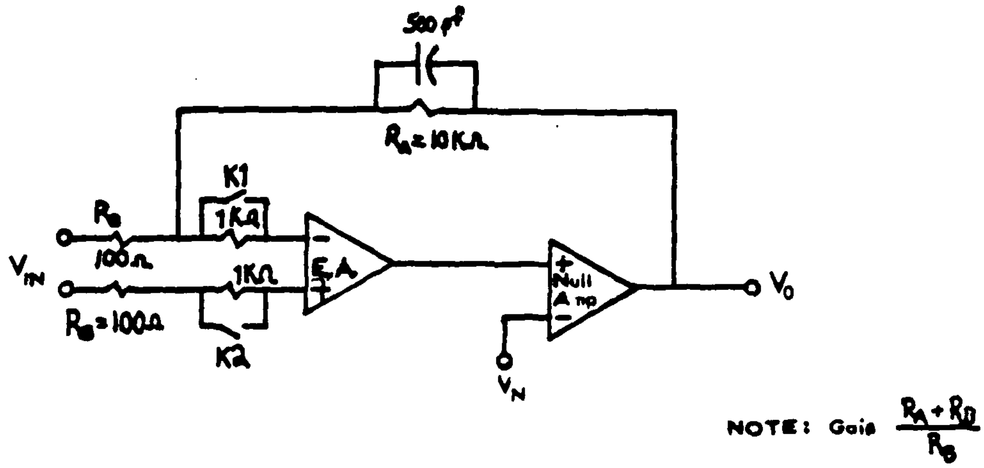


Figure 7-3 Error Amplifier Test Circuit

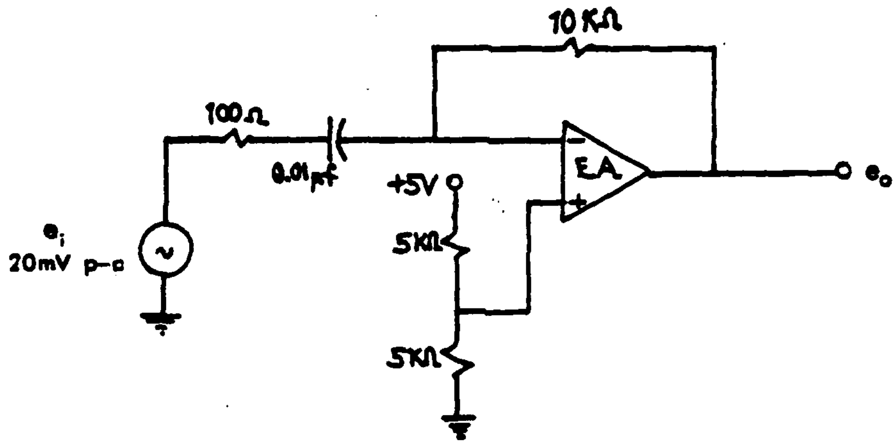


Figure 7-4 Unity Gain Bandwidth Test Cicuit

occurs is the Unity Gain Bandwidth. An alternative method of obtaining G_{BW} is to apply the minimum limit frequency in e_i and measure the magnitude of e_o; if e_o is greater than or equal to e_i the device passes. This method allows the test to be performed by ATE.

Reference:

Since many of the internal elements of the device are dependent on the reference voltage, a special effort was made to perform thorough testing to insure stability and accuracy. The reference voltage V_{REF} is determined by measuring the voltage on the reference pin, with only ground and V_{CC} applied to the device.

Line regulation is found by measuring the difference in the reference voltage when the power supply is varied between 8V and 40V for device type 01 (8V and 35V for device types 02-04). The load regulation measurement is performed in the same way, however, the power supply is held constant and the load current on the reference is varied between 20mA and 0mA. The short circuit limit I_{OS} is determined by grounding the reference and measuring the current flow out of the reference.

The two remaining tests in the reference section are ripple rejection and output noise (N_O). The ripple rejection is determined by adding a 1 V_{RMS}, 2400Hz sine wave to the supply voltage, and the change in V_{REF} is measured to give $\Delta V_{IN}/\Delta V_{REF}$. For frequency components between 10Hz and 10KHz, the noise is found using a filter to block the unwanted frequency on a noise analyzer.

Oscillator:

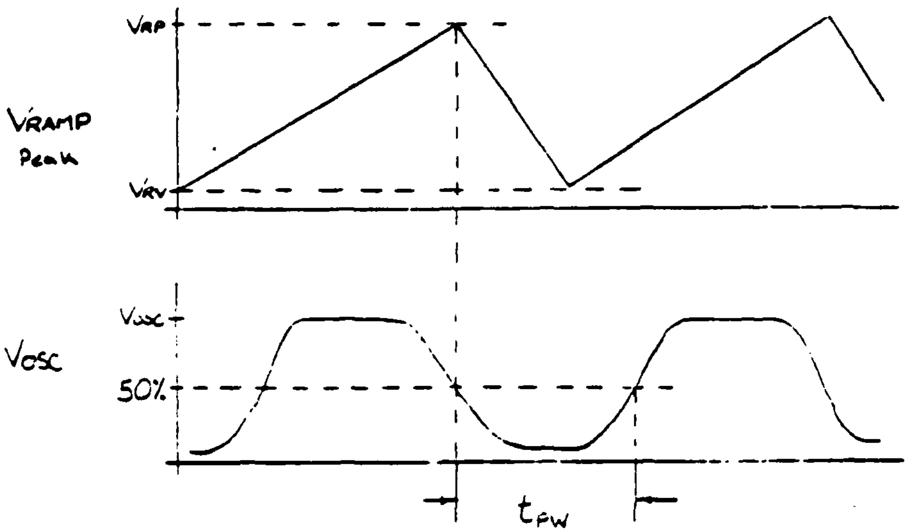
The initial frequency test is used to determine how well the device functions in its normal operating range. This frequency (50KHz for device type 01, 40KHz for device types 02-04) is used for the various tests in the oscillator section, such as initial frequency, voltage and temperature stability, ramp voltage and clock pulse

width. The initial frequency (fosc) is measured using a precision timing resistor and capacitor; both components must be within +/- 0.1% of the specified value. The timing capacitor should be polystyrene, tuned with a mica capacitor for standardization of the components. For device type 03, a 40KHz output frequency is considered a critical frequency for testing. Since the output in the 03 device is twice the frequency of the oscillator, it was determined that the frequency should be measured at the output rather than at the oscillator. The testing of the 01, 02, and 04 device types was performed on the output of the oscillator. For these devices, there is a one to one correspondence between the oscillator and output frequencies. Due to this relationship and the fact that the output requires a greater number of connections in order to function, the oscillator output was chosen for frequency measurements. The capacitor and resistor are chosen in the same manner to measure the minimum and maximum frequencies.

The initial oscillator frequency limit for the 1524 device is specified over a large range (47KHz to 58KHz at $25^{o}C$) and is a result of the differences in frequencies between the various vendors. On the average the devices from each vendor showed good accuracy, with a frequency distribution of 3 to 4 percent around the center frequency. (For example, a particular manufacturer has a center frequency of 50KHz and a range of values between 47.5KHz and 52.5KHz. Another has a center frequency of 56KHz and a range of 54.5KHz to 57.5KHz, with the remainder of the manufacturer devices between these two ranges.)

The voltage stability test fosc/ V_{IN}, as the name implies, examines the effect that power supply variations have on the initial frequency. The supply voltage is varied over the full range, and the change in frequency measured. Clock pulse width t_{pw} for the 1526 device (as shown in Figure 7.5a) is measured from the midpoint of the falling edge to the midpoint of the rising edge.

A. Ramp And Oscillater Voltage



B. Output Rise And Fall Time

Output A, B

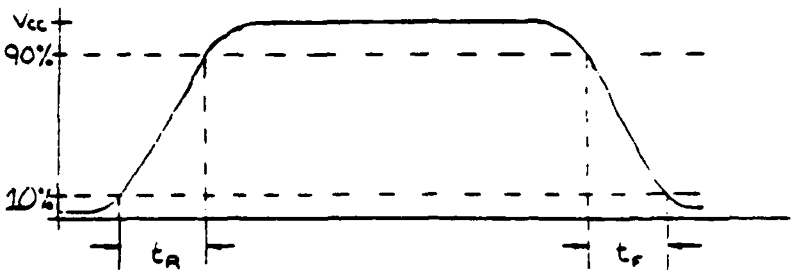
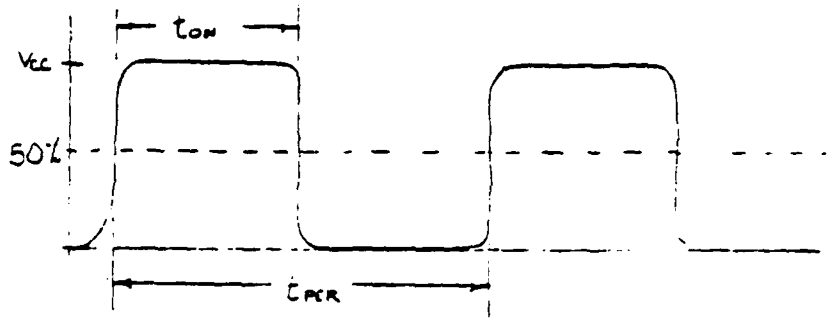


Figure 7-5 Circuit Waveforms

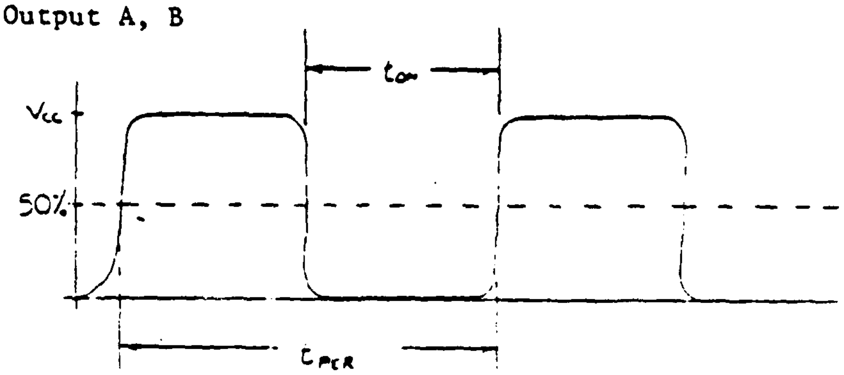
C. Maximum Duty Cycle

Output A, B



Device Type 02, 03

Output A, B

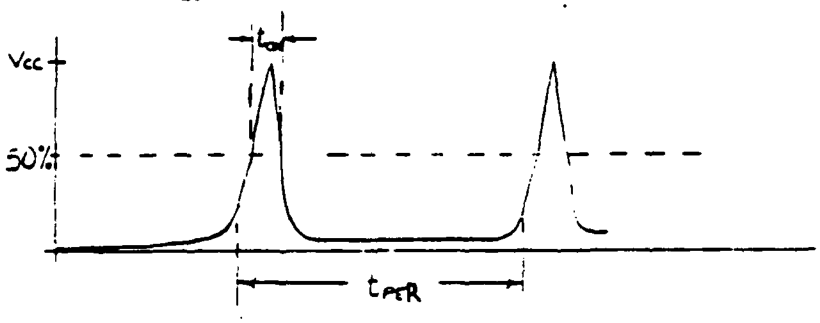


Device Type 01, 04

Figure 7-5 (cont.) Circuit Waveforms

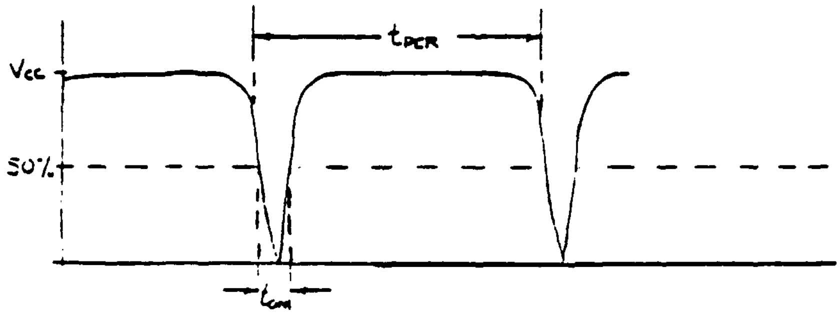
D. Minimum Duty Cycle

Output A, B



Device Type 02, 03

Output A, B



Device Type 04

Figure 7-5 (cont.) Circuit Waveforms

E. Shut-Down Delay

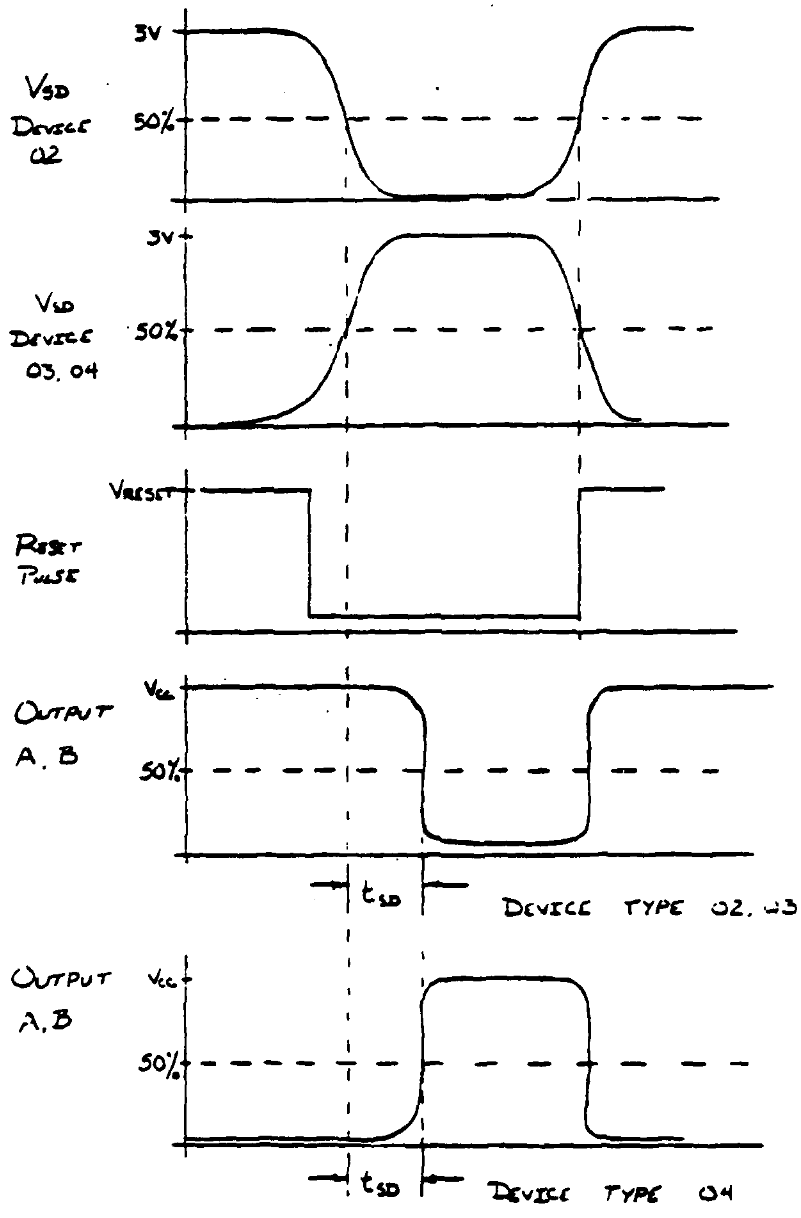


Figure 7-5 (cont.) Circuit Waveforms

F. Synchronization Test

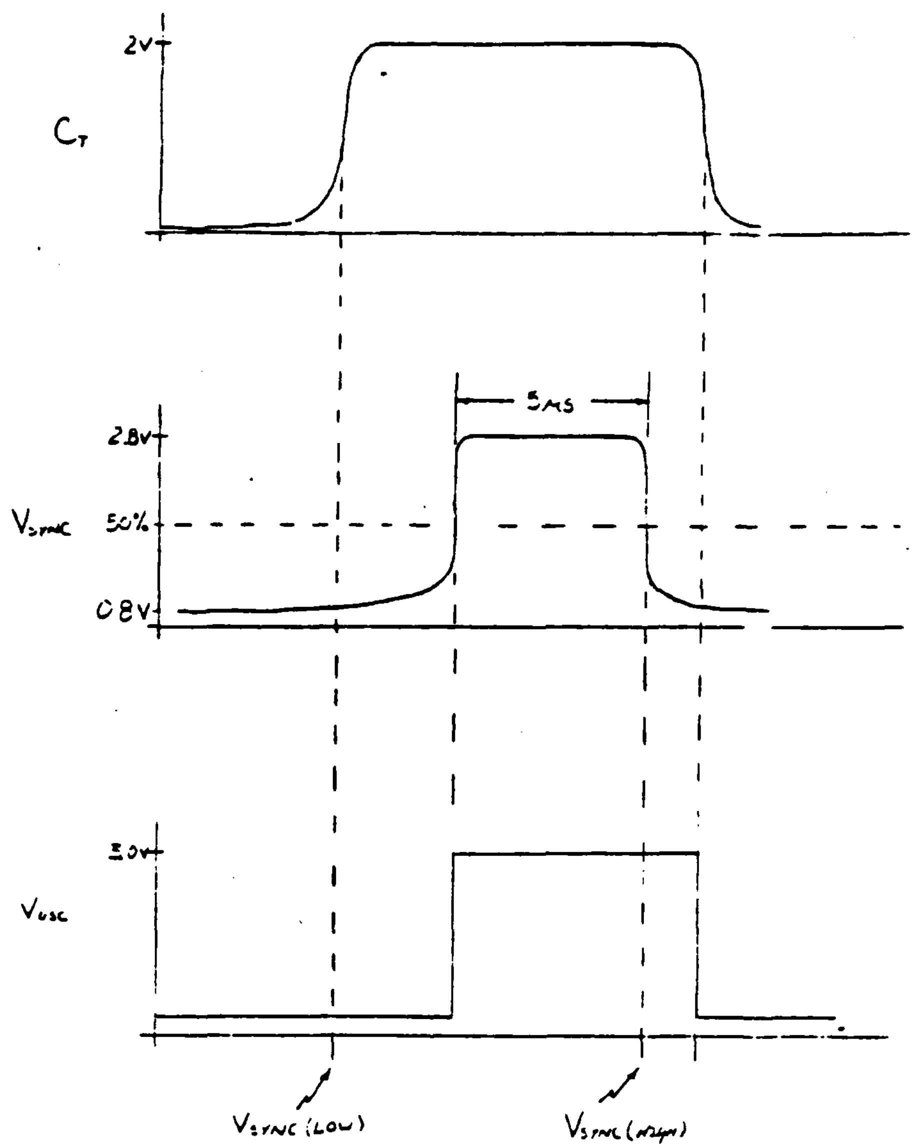


Figure 7-5 (cont.) Circuit Waveforms

For the other three device types, the clock waveform is inverted. The final test is ramp voltage which is determined by examining the waveform on the timing capacitor pin shown also in Figure 7.5a. The valley voltage (V_{RV}) is measured from the 0 volt reference point to the minimum value of the waveform. The peak voltage (V_{RP}) is measured from 0 to the maximum value obtained by the wave.

Output:

The output section tests are as follow: rise and fall time, collector current and output high and low voltages. The rise and fall times are measured on both outputs A and B (shown in Figure 7.5b) and are denoted as T_R and T_F. The circuit requires that the timing resistor and capacitor be connected together, and includes a pull up resistor on the collector of the output transistor. The error amplifier is forced high to minimize its effects. As can be seen in the figure, the T_R is measured from the 10% point to the 90% point and T_F is from 90% to 10% point.

Collector current I_C is the amount of current flow into the output transistors while in the "ON" state. For the 02, 03 and 04 devices, the output transistors are totem poled together, therefore, there is only one measurement. For device type 01, two separate measurements are required. The two remaining tests are output high V_{OH} and output low V_{OL} voltages which are also referred to as emitter output voltage and saturation voltage, respectively. The timing components are not connected for either test. For output high, the output being measured is turned "ON" by toggling the oscillator with a 5 volt 50uS pulse occurs. Output low requires the output to be in the "OFF" state. This is accomplished by toggling the oscillator or, in the case of the 1526, by applying ground to the shut down pin. Both tests are performed with a 20mA and a 100mA load on the outputs, (1524 uses a 50mA load).

Comparator:

The duty cycle adjust range t_{ON}/t_{OSC} in the comparator section is determined by placing the device in a fully functional state. The timing resistor R_T and capacitor C_T are connected, the two inputs to the error amplifier are set equal to the same value within the common mode range, and V_C is set to the supply voltage. The duty cycle range is obtained by setting the voltage on the comparator input to 0.5 volts and measuring the period of the output (t_{OSC}) and the time in the "ON" state (t_{ON}). This will give the minimum duty cycle (shown in Figure 7.5d) equal to t_{ON}/t_{OSC}. If the device is working properly, the transistor should not be ON, and therefore, t_{ON} will equal zero. The maximum duty cycle is determined by setting the comparator input to 3.6 volts. The output will be in the "ON" state for half of the cycle which results in a duty cycle of 50% (as shown in Figure 7.5c).

The final test common to each device type is power supply current (I_{in}). The test is performed by applying the maximum recommended voltage to the device and recording the input current.

The following tests are unique to the particular device types:

Device Type 01:

The current limit sense voltage (V_{SEN}) is determined by grounding the minus input of the current limit amplifier and varying the input on the plus input until the compensation pin reads 2 volts. This is the trigger point of the current limit amplifier which is defined as V_{SEN}. Shutdown voltage tests are go/no-go type testing, where the actual trigger point is not located. The limit is applied and the response is examined. The shutdown voltage high $V_{SD(HI)}$ is measured by applying 1.4 volts to the SHUTDOWN pin and examining the compensation pin. If V_{comp} is less than or equal to 0.5 volts then $V_{SD(HI)}$ passes and the device is shutdown. $V_{SD(LO)}$ is measured by applying 0.4 volts to the SHUTDOWN pin; if V_{comp} is greater than or equal to 3.6 volts, then $V_{SD(LO)}$ passes.

Device Types 02 and 04:

Soft start current (I_{SS}) is determined by grounding the SOFT START and SHUTDOWN pins and measuring the current flow in the soft start. Soft start voltage (V_{SS}) is determined by applying 2 volts to the SHUTDOWN pin and measuring the Soft Start pin.

Shutdown current (I_{SD}) is measured with 2.5 volts connected to the SHUTDOWN pin. Shutdown voltage (V_{SD}) measurement require the timing component to be placed in the circuit, 3.6 volts on the compensation pin, and 20 volts on V_C (pin 13). $V_{SD(LO)}$ is determined by applying 0.5 volts to the shutdown pin and examining both outputs. For device 02, if either output is greater than 2.5 volts, $V_{SD(LO)}$ passes. (For device 04 - VSD (LO) passes if either output is less than 2.5 volts). $V_{SD(HI)}$ is determined by applying 1.6 volts to the SHUTDOWN pin. Device 02 passes if both outputs are less than 2.5 volts. (For device 04 to pass, both outputs must be greater than 2.5 volts).

Device Type 03:

Under-voltage lockout (V_R) is measured to determine if the device turns off when the voltage on the reference drops to low. The supply voltage (V_{IN}) and reference (V_{REF}) pins are connected together, for $V_{R(LOW)}$ the two are set to 3.8 volts and the voltage on the reset is measured. A value less than 0.4V indicates the device is turned off. For $V_{R(HIGH)}$, V_{IN} and V_{REF} terminals are set to 4.8 volts and the reset pin again measured. A value greater than 2.4V indicates the device is active.

The 1526 possesses three digital ports called SYNC, RESET and SHUTDOWN. The following parameters for these parts are evaluated: input current high and low (I_{IH}, I_{IL}) and output voltage high and low (V_{OHP}, V_{OLP}). The three ports are tested

in a similar manner. The current limit amplifier inputs are grounded for all twelve tests. For I_{IH}, 2.4 volts are applied to the port and the current flow into the device is measured. For I_{IL}, 0.4 volts are applied to the particular port and the current measured. The only difference exists for the current tests on the SYNC pin which requires the timing capacitor pin to be less than or equal to 0.5 volts. V_{OHP} is determined by forcing a -40uA current into the port and measuring the voltage. For V_{OLP}, apply 3.6mA to the port and measure the voltage. For the SHUTDOWN port, V_{OLP} requires the positive input of the current limit comparator to be placed at 120mV and the negative input at ground. The difference on the comparator will cause the shutdown to be driven low. A voltage greater than 3.6 volts on the timing capacitor pin is required to force the V_{OLP} SYNC low.

The capacitor charging current I_{CS} is the amount of current in the SOFT START terminal C_{SS}. To determine I_{CS}, the C_{SS} pin is grounded and the current flow is measured. The Error clamp voltage V_{EC} test is performed by applying 0.4V to the RESET pin and measuring the voltage which appears of the C_{SS} pin.

The remaining tests, sense voltage V_S and Input Bias Current I_{IBS}, pertain to the current limit comparator. The sense voltage is the amount of voltage at the positive input of the comparator required to activate the output. The value is obtained by grounding the negative input of the current limit comparator and increasing the voltage on the positive input until the voltage at the SHUTDOWN pin is less than 0.4V. The voltage which causes the SHUTDOWN to switch is V_S. The input bias current is measured at both the positive ($+I_{IBS}$) and negative ($-I_{IBS}$) current values by taking the current reading referenced to ground.

The burn-in circuit design for all four device types required many iterations due to their high power consumption. With the burn-in temperature specified at 125°C, and the maximum recommended power supply voltage, the devices would exceed

their maximum allowable junction temperature. The burn-in circuit for device type 03 is shown in Figure 7.6. The other three are almost identical and, therefore, are not pictured. In order to alleviate the problem of excessive junction temperature, the recommended supply voltage for device type 02, 03 and 04 were lowered. The supply voltage for the 02 and 04 are set to 30 volts for class B and 27 volts for class S devices; the 03 are set to 20 volts maximum recommended. The operation from 8 volts to 35 volts is allowed if care is taken not to exceed the maximum junction temperature (this might require the uses of a heat sink in some instances). The higher voltage is also allowed in some of the parameter testing, such as for the short period of time when measuring total supply current.

As a result of the testing and discussions with manufacturers, test condition and limits were determined. The tests limits are shown in Table 7.4 for all four device types.

An example of LTX device data for the 1524 is shown in Table 7.5. Due to the large volume of similar data, only a sample is shown here. The timing tests not shown in the printout were performed with a bench top test circuit and all of the devices were within their specified limits.

7.5 CONCLUSIONS AND RECOMMENDATIONS

The test data obtained from the various manufacturer's devices indicates that the regulating pulse width modulators will meet all of the specifications set forth in MIL-M-38510/126A. However, the following two issues are of great concern regarding device operation in a circuit:

a. For device type 01, care must be taken if the frequency of the output is critical since a substitution of a different vendor's device could cause an unacceptable frequency shift.

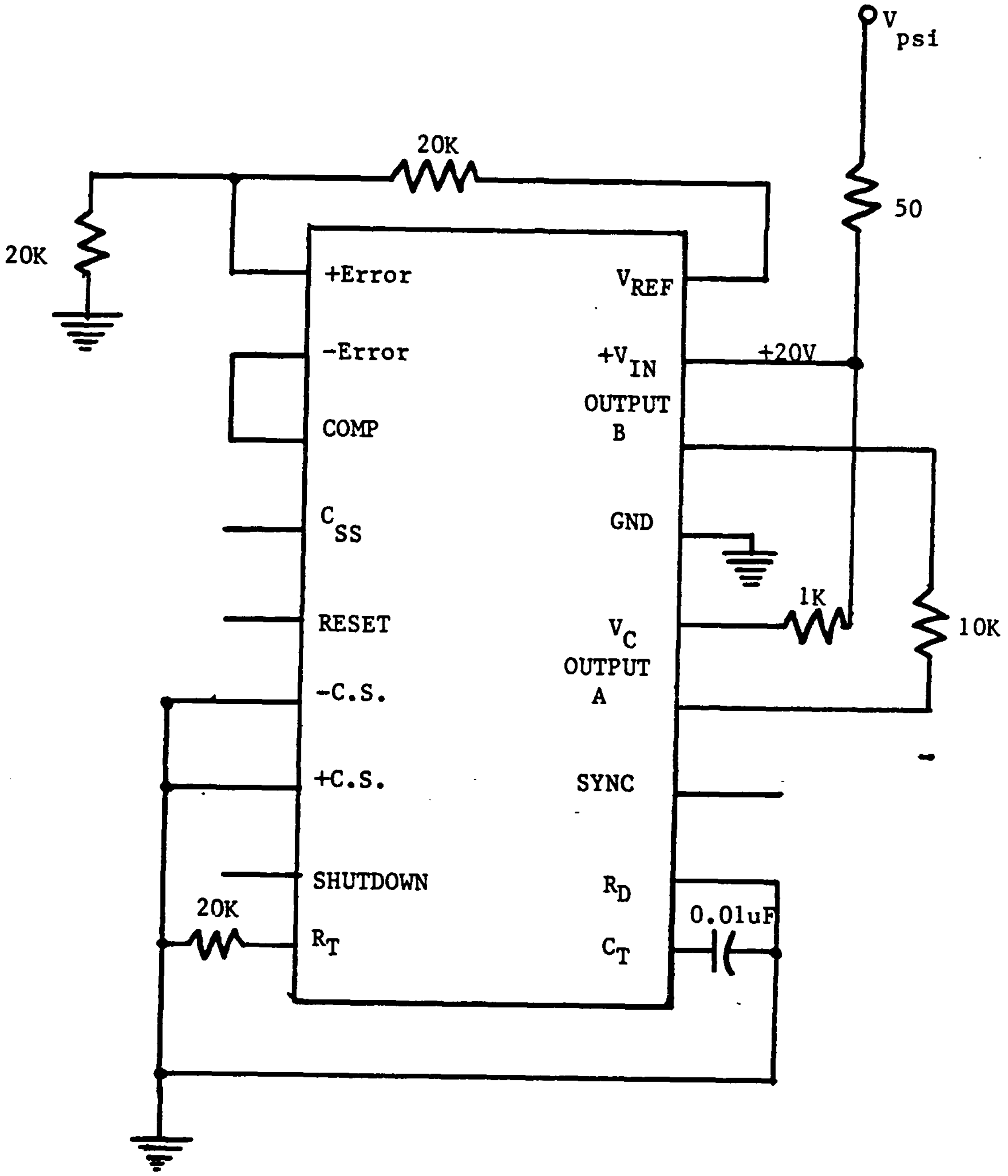


Figure 7-6 Burn-In Circuit 1526

Characteristic	Symbol	Condition VIN=20v RT=2 Kohms +/-0.1% CT=0.01uF +/-0.1% (Unless otherwise specified) -55 C <= Tc <= 125 C	Limits MIN	 MAX	Units
ERROR AMPLIFIER:					
Input offset voltage	VIO	VCM= 2.5v	-5	5	mV
Input bias current	IIB	VCM= 2.5v	.01	10	uA
Input offset current	IIO	VCM= 2.5v	-1	1	uA
Compensation current (sink)	ICOS1	VIN(I)-VIN(NI) >=150mV TC=25 deg C	65	170	uA
Compensation current (source)	ICOS2	VIN(NI)-VIN(I) >=150mV TC=25 deg C	-170	-65	uA
Common mode rejection	CMR	1.8v <= VCM <= 3.4v	70	---	dB
Open loop voltage gain	AVS	TC=25 deg C	72	---	dB
		TC=-55 deg C, 125 deg C	68	---	dB
Unity gain bandwidth	GBW	TC=25 deg C	3	---	MHz
REFERENCE:					
Output voltage	VREF		4.8	5.2	V
Line regulation	VRLINE	8v <= VIN <= 40v	-20	20	mV
Load regulation	VRLOAD	-20mA <= IREF <= 0	-50	50	mV
Ripple rejection	ΔVIN/ ΔVREF	VIN=20v ei=1Vrms f=2400 Hz TC=25 deg C	50	---	dB
Short circuit current limit	IOS 1/	t <= 25ms TC=125 deg C	-120	---	mA
		VREF=0v TC=-55,25 deg C	-190	---	mA
Output noise voltage	NO	TC=25 deg C 10Hz <= f <= 10KHz	---	200	uVrms
OSCILLATOR:					
Maximum frequency	fOSC (max)	RT=2 KOhms +/-0.1% CT=0.001 uF +/-1.0%	250	---	KHz
Initial frequency	fOSCI	TC=25 deg C	47	58	KHz
Oscillator	fOSC2	TC= 125 deg C	45	60	KHz
Frequency	fOSC3	TC= -55 deg C	45	60	KHz
Frequency change with voltage	ΔfOSC1/ΔVIN	8 V<=VIN<=40 V,TC=25 deg C	-2	2	%
Output amplitude	VOSC		2.4	--	V
Output pulse width	Tpw		0.3	--	uS
Ramp voltage	VRAMP		3.0	3.8	V
Saturation voltage	VSAT (osc)	ICT=5mA,VOSC= 5 V, TC= 25 deg C	0.7	1.1	V
COMPARATOR:					
Duty cycle adjust range	tON/tOSC 2/	Min value: Vcm=2.5 Vcomp= 0.5V	---	0.001	%
		Max value: Vcm= 2.5V Vcomp= 3.8V	45	50	%

Device Type 01
TABLE 7-4 Electrical Parameter Limits

Characteristic	Symbol	Condition VIN= 20V RT=2 KOhms +/-0.1% CT=0.01uF +/-0.1% (Unless otherwise specified) -55 C <= Tc <= 125 C	Limits MIN	MAX	Units
OUTPUT SECTION: 3/					
Collector leakage current	ICEX	VC = 40V	--	10	uA
Saturation voltage	V(SAT)	VIN(NI)-VIN(I)>=150mV IC = 50mA,	--	2	V
Emitter output voltage	VEO	VIN(NI)-VIN(I) >=150mV TC= 25 deg C, VC=20V, IE = -50mA	17	--	V
Rise time	TR(tr)	VIN(NI)-VIN(I)>=150mV RC= 2 KOhms, VC=20V, TC=25 deg C, CL=15pF	--	0.4	uS
Fall time	TR(tf)	VIN(NI)-VIN(I)>=150mV RC= 2 kOhms,VC=20V, TC=25 deg C, CL= 15pF	--	0.2	uS
SHUT DOWN CIRCUIT:					
Sense voltage	VSEN	VIN(NI)-VIN(I)>=150mV VEOA= 2V, TC=25 deg C	190	210	mV
		TC= 125 or -55 deg C	165	235	mV
		--			mV
Shutdown 4/	VSD (high)	VIN(NI)-VIN(I)>=150mV	1.4	--	V
	VSD (low)	VIN(NI)-VIN(I)>=150mV	--	0.4	V
TOTAL STANDBY CURRENT:					
	IIN	VIN = 40 V,	--	10	mA

1/ Continuous short circuit limits will be less than indicated test limits.
2/ tOSC is the period of the output waveform.
3/ Each output transistor shall be tested for all parameters listed.
4/ This is a go-nogo test, the limit values are used for input voltages.

Device Type 01
TABLE 7-4 Electrical Parameter Limits

Characteristic	Symbol	Conditions VIN= 20V dc,RT=3.6KOhms+0.1% RD=0 Ohms,CT=0.01uF+0.1% -55 C <= TC <= 125 C (Unless Otherwise Specified)	Limits Min	Max	Units
REFERENCE SECTION:					
Output voltage	VREF	TC=-55 deg C,125 deg C	5	5.2	V
		TC=25 deg C	5.05	5.15	V
Line Regulation	VRLINE	VIN= 8V to 35V	-30	30	mV
Load Regulation	VRLOAD	IREF = 0 to 20mA	-50	50	mV
Short Circuit Current	IOS 1/	VREF =0V, t<=25mS	-125	--	mA
Output Noise Voltage	NO	10 Hz<=f<=10KHz TC= 25 deg C	--	200	uVRMS
Ripple Rejection	ΔVIN / ΔVREF	VIN= 20V+1VRMS f=2400Hz TC= 25 deg C	50	--	dB
OSCILLATOR SECTION:					
Initial Frequency	fOSC	TC= 25 deg C	37.5	42.5	KHz
Saturation Voltage	VSAT (OSC)	IDIS= 5mA,VOSC= 5V TC= 25 deg C	0.5	1.1	V
Oscillator-Frequency	fOSC2	TC= -55 deg C	36	44	KHz
Clock Amplitude	VOSC		3.0	--	V
Clock Pulse Width	Tpw	TC=25 C, -55 deg C	0.3	1.0	uS
		TC= 125 deg C	0.3	1.4	uS
Ramp Voltage	VRAMP		3.0	3.6	V
Voltage Stability	ΔfOSC	VIN= 8 to 35V,TC= 25 deg C	-1	1	%
Minimum Frequency	fOSC (min)	RT= 150KOhms +0.1% CT= 0.1uF +1.0%,RD=0 Ohms	--	150	Hz
Maximum Frequency	fOSC (max)	RT= 2KOhms +0.1% CT= 0.001uF +1.0%,RD=0 Ohms	300	--	KHz
Sync	VSYNC (LO)		--	0.8	V
	VSYNC (HI)		2.8	--	V
Sync Input Current	ISYNC	Sync Voltage= 3.5V	--	2.5	mA
ERROR AMPLIFIER SECTION:					
Input Offset Voltage	VIO		-5	5	mV
Input Bias Current	IIB		.01	10	uA
Input Offset Current	IIO		-1	1	uA
Open Loop Voltage Gain	AVS	VCM= 2.5 V	60	--	dB
Common Mode Rejection Ratio	CMMR	VCM = 1.5V to 5.2V	60	--	dB
Supply Voltage Rejection Ratio	SVRR	VIN = 8V to 35V	60	--	dB
Unity Gain Bandwidth	GBW	AV= 0dB,see fig. 8 TC=25 deg C	2	--	MHz
Output High Level	VHI		3.8	--	V
Output Low Level	VLO		--	0.5	V

Device Type 02,04

TABLE 7-4 Electrical Parameter Limits (Cont.)

Characteristic	Symbol	Conditions VIN= 20V dc RT=3.6KOhms+/-0.1% RD=0 Ohms CT=0.01uF+/-0.1% -55 C <= TC <= 125 C (Unless Otherwise Specified)		Limits MIN	MAX	Units
P.W.M. COMPARATOR SECTION:						
Maximum Duty Cycle	tON(max) / tOSC	2/ VCOMP= 3.6V		45	50	%
Minimum Duty Cycle	tOSC(min) / tOSC	2/ VCOMP= 0.6V		--	0.001	%
OUTPUT SECTION: 3/						
Output Low	VOL	ISINK= 20mA		--	0.4	V
	VOL	ISINK= 100mA		--	2	V
Output High	VOH	ISOURCE= 20mA		18	--	V
	VOH	ISOURCE= 100mA		17	--	V
Under Voltage Lockout	VUL			6	8	V
Shutdown Delay	tSD	VSD= 3V	TC= 25 deg C, -55 deg C	--	500	nS
			TC= 125 deg C	--	700	nS
Rise Time	TR(tr)			--	600	nS
Fall Time	TR(tf)			--	300	nS
VC Standby Current	IC	VC= 35V		--	200	uA
SOFT START SECTION:						
Soft Start Current	ISS	VSD= 0V		-80	-25	uA
Shutdown Input Current	ISD	VSD= 2.5V		--	1	mA
Soft Start Voltage	VSS	VSD= 2V		--	0.6	V
Shutdown Voltage	VSD(LO)			--	0.5	V
	VSD(HI)			1.6	--	V
Total Supply Current	IIN	VIN= 35V	TC=-55, 25 deg C	--	20	mA
			TC= 125 deg C	--	18	mA

Note:
1/ Continuous Short Circuit Limits will be less then indicated test limits.
2/ tOSC is the period of the output waveform.
3/ Each output transistor shall be tested for all parameters listed. VC= 20V unless otherwise specified.

Device Type 02,04

TABLE 7-4 Electrical Parameter Limits (Cont.)

Characteristic	Symbol	Conditions VIN= 15V dc,RT=4.12KOhms+0.1% RD=0 Ohms CT=0.01uF +0.1% -55 C <= TC <= 125 C (Unless otherwise specified)	Limits MIN	 MAX	Units
REFERENCE SECTION:					
Reference Output Voltage	VREF		4.90	5.10	V
Line Regulation	VRLINE	VIN= 8V to 35V	-20	20	mV
Load Regulation	VRLOAD	ILOAD= 0mA to 20mA	-30	30	mV
Short Circuit Current	IOS 2/	VREF= 0V t<= 25mS	-125	--	mA
Output Noise Voltage	NO	10Hz<=f<=10 KHz, Tc=25 deg C	--	200	uVRMS
Ripple Rejection	$\frac{\Delta VIN}{\Delta VREF}$	VIN= 15V+1VRMS,TC=25 deg C Sinewave @2.4KHz	50	--	dB
OSCILLATOR SECTION: 5/					
Initial Frequency	fOSC	TC= 25 deg C	38	42	KHz
Voltage Stability	ΔfOSC	8V<= VIN<=35V	-1	1	%
Oscillator Frequency	fOSC1	TC= 125 deg C, -55 C	36	44	KHz
Minimum Frequency	fOSC (MIN)	RT= 150 KOhms +0.1% CT= 0.20uF +1.0%,RD=0 Ohms	--	100	Hz
Maximum Frequency	fOSC (MAX)	RT= 2 KOhms +0.1% CT= 1.0nF +1.0%,RD=0 Ohms	350	--	KHz
Clock Width	Tpw	TC= 25 deg C, -55 C	--	2	uS
		TC= 125 deg C	--	3	uS
Sawtooth Peak Voltage	VRP	VIN= 35V	2.5	3.5	V
Sawtooth Valley Voltage	VRV	VIN= 8V	0.45	--	V
ERROR SECTION:					
Input Offset Voltage	VIO	VCM= 2.5V	-5	5	mV
Input Bias Current	IIB	VCM= 2.5V	-1	--	uA
Input Offset Current	IIO	VCM= 2.5V	-0.5	0.5	uA
Open Loop Voltage Gain	AVS		60	--	dB
Common Mode Rejection Ratio	CMRR	VCM= 0 to 5.2V	70	--	dB
Supply Voltage Rejection Ratio	SVRR	VIN= 8V to 35V,VCM=2.5V	66	--	dB
Unity Gain Bandwidth	GBW	See Fig.8, TC=25 degC,AV=0dB	3	--	MHz
Output High Level	VHI	Vpin1- Vpin2>=150mV, ICOMP= -100uA	3.6	--	V
Output Low Level	VLO	Vpin1- Vpin2>=150mV, ICOMP= 100uA	--	0.4	V
P.W.M. COMPARATOR:					
Maximum Duty Cycle	$\frac{tON(MAX)}{tOSC}$	1/ VCOMP= 3.6V	45	50	%
Minimum Duty Cycle	$\frac{tON(MIN)}{tOSC}$	1/ VCOMP= 0.4V	--	0.001	%

Device Type 03
TABLE 7-4 Electrical Parameter Limits (Cont.)

Characteristic	Symbol	Conditions VIN= 15V dc RT=4.12KOhms+/-0.1% RD=0 Ohms CT=0.01uF+/-0.1% -55 C <= TC <= 125 C (Unless otherwise specified)	Limits MIN	MAX	Units
OUTPUT DRIVERS: 3/					
Saturation Voltage	VCE	VC= 15V, ISINK= 20mA	--	0.3	V
		ISINK= 100mA	--	2.0	V
Output High	VOH	VC= 15V, ISOURCE= 20mA	12.5	--	V
		ISOURCE= 100mA	12.0	--	V
Shutdown Delay	tSD	VC=15V TC= -55 C, 25 C	--	0.5	uS
		TC= 125 deg C	--	0.7	uS
Rise Time	tR	VC= 15V	--	0.3	uS
Fall Time	tF	VC= 15V	--	0.2	uS
VC Standby Current	IC	VC= 35V	--	150	uA
DIGITAL PORTS: SYNC RESET SHUTDOWN 4/					
High Input Current	IIH	VIH= 2.4V	-200	--	uA
Low Input Current	IIL	VIL= 0.4v	-360	--	uA
High Output Voltage	VOHP	ISOURCE= 40uA	2.4	--	V
Low Output Voltage	VOLP	ISINK= 3.6mA	--	0.4	V
CURRENT LIMIT COMPARATOR:					
Sense Voltage	VS		80	120	mV
Input Bias Current	IIBS		-10	--	uA
SOFT START SECTION:					
Error Clamp Voltage	VEC		--	0.4	V
Capacitor Charging Current	ICS		-150	-50	uA
UNDER VOLTAGE LOCKOUT:					
Reset Output(Low) Voltage	VR (LOW)	VREF= 3.8V	--	0.4	V
Reset Output(High) Voltage	VR (HIGH)	VREF= 4.8V	2.4	--	V
POWER CONSUMPTION:					
Standby Current	IIN	SHUTDOWN= 0.4V VIN= 35V			
		TC= -55, 25 deg C	--	30	mA
		TC= 125 deg C	--	25	mA

Notes:

1/ tOSC is the period of the output waveform in this case.
2/ Continuous Short Circuit limits will be less than indicated test limits.
3/ Each output transistor shall be tested for all parameters listed VC= 15V unless otherwise specified.
4/ Only use the shutdown pin to deactivate the device do not use the Sync pin.
5/ A 2.7 KOhms pull-up resistor is added to the Sync pin to limit stray capacitance in automatic test equipment.

Device Type 03

TABLE 7-4 Electrical Parameter Limits (Cont.)

TEST 100			
100.0	25.0	DGR	TEST TEMPERATURE
TEST 1			
1.0	4.05	MA	ICC AT 40V
TEST 2			
2.0	5.01	V	VREF AT VIN=20V
TEST 3			
3.0	7.60	MV	LINE REG 8-40V
TEST 4			
4.0	-32.52	MV	LOAD REG 0-20MA VIN=20V
TEST 5			
5.0	-34.96	MA	ISC- REF
TEST 6			
6.0	0.05	UA	COLLECTOR LEAKAGE AT 40V- XSISTOR 'A'
TEST 7			
7.0	0.06	UA	COLLECTOR LEAKAGE AT 40V- XSISTOR 'B'
TEST 8			
8.0	1.39	V	VSAT AT 50MA- XSISTOR 'A'
TEST 10			
10.0	17.50	V	EMITTER HI XSISTOR 'A'
TEST 9			
9.0	1.39	V	VSAT AT 50MA- XSISTOR 'B'
TEST 11			
11.0	17.78	V	EMITTER HI XSISTOR 'B'
TEST 12			
12.0	0.21	MV	VIO
TEST 13			
13.0	1.75	UA	IBIAS (EA)
TEST 14			
14.0	0.37	UA	IIO (EA)
TEST 15			
15.0	4.23	V	+SWING (EA)
TEST 16			
16.0	0.08	V	-SWING (EA)
TEST 17			
17.0	99.7	UA	COMP I LO (REF)
TEST 18			
18.0	-102.9	UA	COMP (REF)
TEST 19			
19.0	-3.17	UA	DELTA COMP (REF)
TEST 20			
20.0	73.9	DB	AVOL
TEST 21			
21.0	63.5	DB	CMRR
TEST 22			
22.0	0.77	V	SHUTDOWN THRESH
TEST 23			
23.0	194.9	MV	CURRENT LIMIT THRESH
TEST 24			
24.0	-1.82	MA	OSC I MIRROR (REF)
TEST 25			
25.0	1.13	V	OSC SAT Q 50MA (REF)
TEST 26			
26.0	4.97	V	OSC CHECK
26.1	2.63	V	OSC CHECK
26.2	2.76	V	OSC CHECK
TEST 27			
27.0	373.5	KHZ	OSC OUTPUT FREQ
27.1	48.0	KHZ	OSC OUTPUT FREQ

Table 7-5 1524 Data Listing

b. When operating devices types 02, 03 and 04 at high voltages, care must be taken not to exceed the maximum junction temperature.

7.6 BIBLIOGRAPHY

a. Silicon General Product Catalog (1986)

b. Applications Handbook, Unitrode (1985-86)

SECTION VIII

SHUNT REGULATING REFERENCE

MIL-M-38510/148

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LIST OF FIGURES

LIST OF TABLES

8.1 INTRODUCTION AND DEVICE DESCRIPTION

This section of the report discusses the characterization effort for the TL431 three terminal programmable shunt regulator diode. The TL431 monolithic voltage reference operates as a low temperature coefficient zener which can be programmed from the range of Vref (2.5V) to 36 volts by two external resistors. Furthermore, the TL431 has a wide operating current range from 1.0mA to 100mA, and a dynamic impedance specification of 0.22 ohms. Characteristics of the reference allows it to replace zenor diodes used in various applications such as power supplies or op-amp designs. The 2.5 volt reference makes it possible to obtain a stable reference from a single 5.0V supply and since the reference operates as a shunt regulator, it can be used as either a positive or negative voltage reference (see Figure 1). The TL431 shunt regulator reference is a multi-sourced device with increasing DOD system usage. Electrical characterization test circuits, test conditions, and limits are specified in MIL-M-38510/148.

TABLE I TABLE OF DEVICE TYPE SPECIFIED

Device	Generic	Manufacturer	Description
01	TL431MJG	Motorola	Programmable Precision Reference

8.2 TEST DEVELOPMENT

A list of the parameters used to electrically characterize the TL431 shunt regulator voltage reference is listed in Table 2.

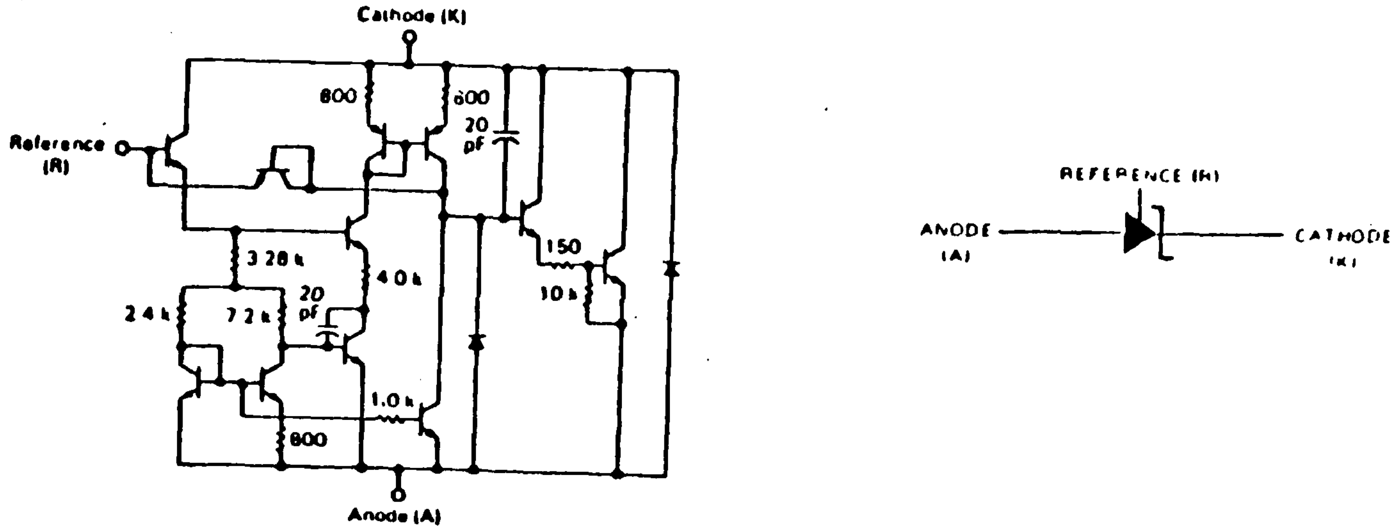


Figure 1 TL431 Schematic and Block Diagram

TABLE 2 CHARACTERIZATION PARAMETERS

Item	Symbol	Parameter
1	V_{ref}	Reference Input Voltage
2	VKA10	Cathode Voltage (10V)
3	VKA36	Cathode Voltage (36V)
4	dVR/dVK	Ratio of Change in VREF to change in VKA
5	IREF	Reference Input Current
6	IMIN	Min Cathode Current for Reg
7	IOFF	Off-State Cathode Current
8	dVR/dT	Reference Voltage Temperature Drift
9	ZKA	Input Impedance
10	No	Noise (0.1 Hz to 10Hz)

Test Circuits:

All dc parametric data was taken off the LTX77 Analog Microcircuit Test System, with the noise measurement being made with a bench-top test fixture. The static test circuits are shown in Figure 2 and the noise test circuit is shown in Figure 3.

8.3 TEST RESULTS AND DISCUSSION

Data obtained from the characterization effort revealed that the part performed very well within the manufacturers specified limits, over all three temperature ranges of $-55^{\circ}C$, $25^{\circ}C$, $125^{\circ}C$.

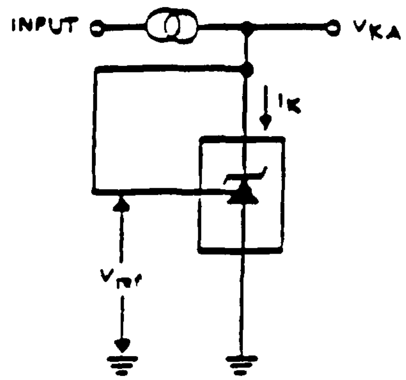


Figure 2a

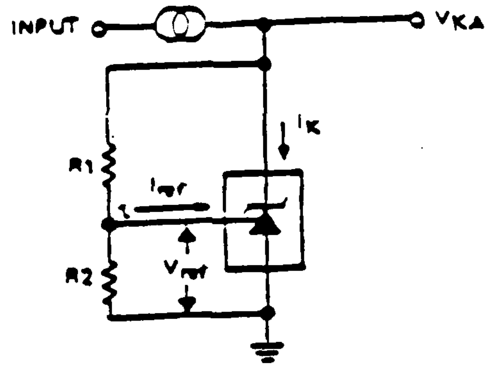


Figure 2b

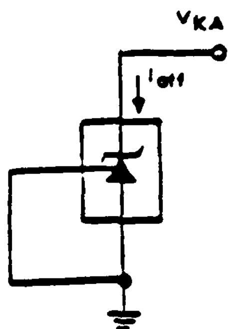


Figure 2c

Figure 2 TL431 Static Test Circuit

Reference Input Voltage (Vref)

The reference input voltage parameter was measured by supplying a known current into cathode of the reference (I_R = 10 mA) and measuring the resultant voltage at that terminal. Data obtained showed that this parameter met the specified limit, with the mean being around 2.47V and the lowest measurement reading 2.466V. See Figure 2a.

Cathode Voltage (10V), VKA10

This parameter was measured by using the circuit shown in Figure 2b with R1 = 10K ohm and R2 = 3.33K ohm and measuring the reference terminal pin 8. Measurements taken revealed that the mean value recorded was approximately 9.85V, with a minimum reading of 9.81V and a maximum reading of 9.90V.

Cathode Voltage (36V), VKA36

The 36V cathode voltage parameter was measured using the same technique as for the VKA10 parameter, except the specified R2 value equals 746 ohms in Figure 2b. All parts passed the specified limit with minimum reading equal to 35.06V and the maximum measurement equal to 35.39V.

Ratio of Change in Vref to Change in VKA, (dVR/dVK)

This measurement was taken at $T_A = 25^{\circ}C$, using the test circuit shown in Figure 2b with R2 equal to 3.33K ohms and R2 = 746 ohms. Results obtained show the amount of variance in the reference voltage with respect to changes in the programmed cathode voltage. All 20 pieces tested passed this parameter, with the greatest variance noted at the programmed VKA voltage of 10V.

Reference Input Current (IREF)

Using the circuit shown in Figure 2b, the reference input current was measured with R1 $=\infty$, and the amount of current inputted into the zener reference was measured with R1 = 10K ohms. This data was taken over all three temperature ranges and all values were well within the specified limit of 4.0uA at ambient and 7.0uA over temperature.

Minimum Cathode Current for Regulation (IMIN)

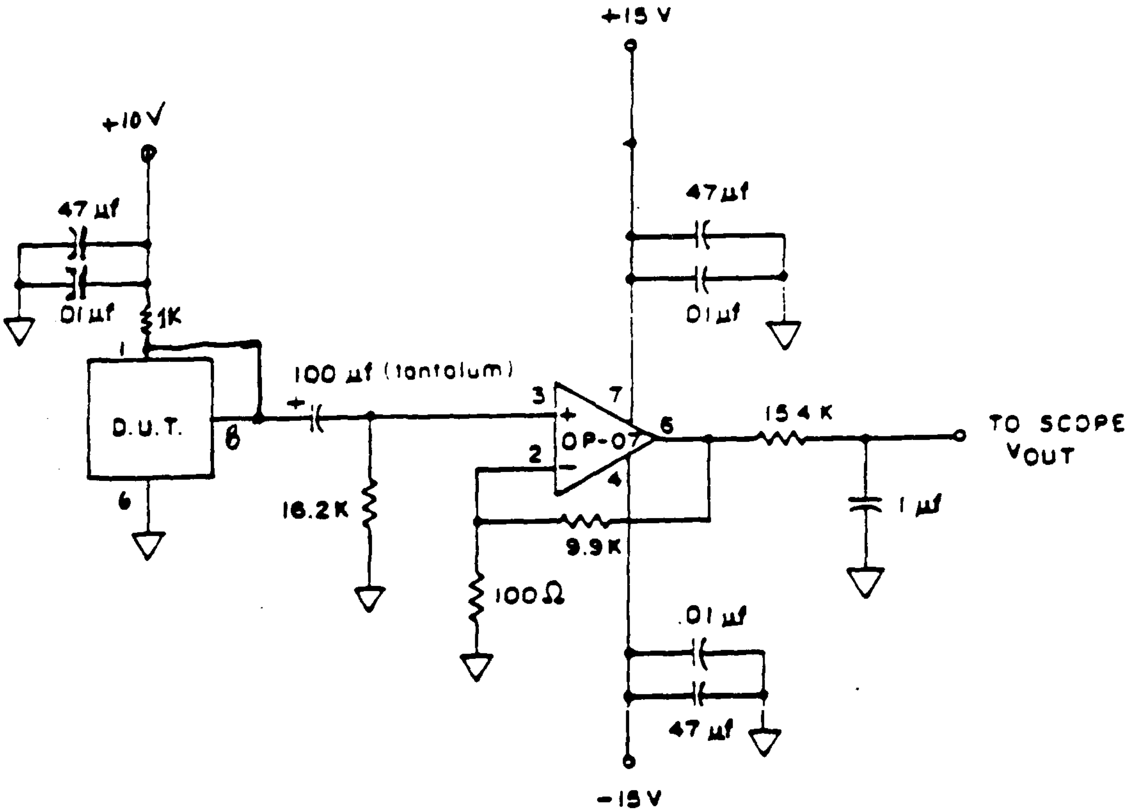
Testing of this parameter is a GO/NO GO test in which a minimum current (IK = 1mA) is supplied into the cathode of the zener. The voltage is then measured to verify that the part is in regulation. All parts passed this parameter over all three temperatues. See Figure 2a.

Off-State Cathode Current (IOFF)

This measurement is taken using the circuit shown in Figure 2c and verifies the amount of leakage current associated with the reverse bias zener diode. All the references tested passed this parameter, over all three temperatures, with the worst case measurements occuring at $T_A = 125^oC$.

Input Impedance (ZKA)

Using the test circuit shown in Figure 2a, the input impedance is measured by supplying two known currents IK = 1mA and IK = 100mA, measuring change in resultant reference voltage, and then dividing this difference by the difference in supplied cathode current. Data obtained shows that the worst case measurement occurred at $T_A = 125^oC$ and was still three orders of magnitude less than the specified limit of 0.5 ohms. All devices passed this test.



NOTES:
1. Test time = 10 seconds.
2. V_{OUT} measured with differential amplifier 7A22 and lower frequency set to 0.1 Hz.

Figure 3 TL431 Low Frequency Noise Test Circuit

Low Frequency Noise (0.1 Hz to 10 Hz), (No)

This test was done on the bench with the circuit shown in Figure 3. Output of the device under test (DUT) was inputted to a low pass filter and then amplified by 100 via the operational amplifier (OP07) gain circuit. The data obtained shows that the nominal value for 1/F noise is 10uV p-p with a deviation of $\pm$5uVp-p. All parts passed the limit of 20uVp-p.

8.4 CONCLUSIONS AND RECOMMENDATIONS

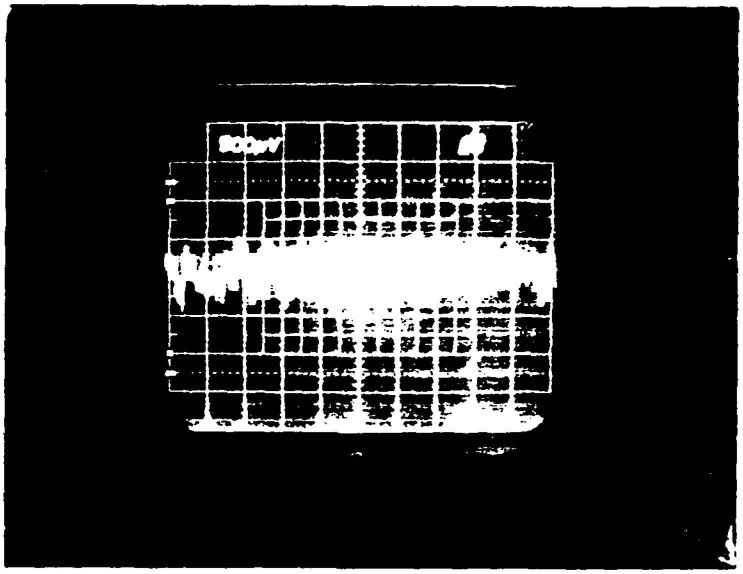
The data obtained from the analyses showed that the shunt regulator reference voltage device met the specifications supplied by the vendor. It is recommended that DOD system designers utilize these devices if screened per MIL-M-38510/148.

8.5 BIBLIOGRAPHY

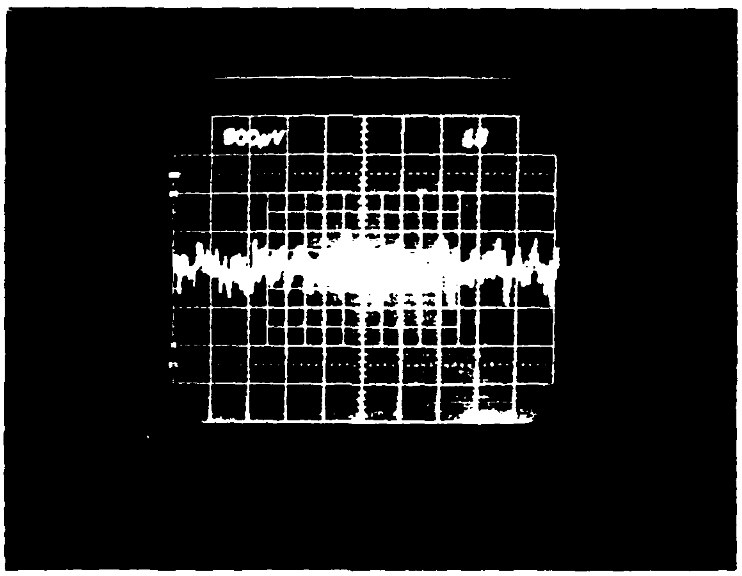
Motorola Semiconductor Data Book

8.6 APPENDIX

The appendix contains: Table I of MIL-M-38510/148, sample test data, and waveforms which are too lengthly for insertion within the text of this report.



SN 14 Low Frequency Noise Output Waveform
(Horizontal Deflection = 5uV/div)
(Vertical Deflection = 1S/div)



SN 17 Low Frequency Noise Output Waveform
(Horizontal Deflection = 5uV/div)
(Vertical Deflection = 1S/div)

Characteristic	Symbol	Conditions $R_1 = 10\ k\Omega$, $I_K = 10\ mA$ (see 3.4) (unless otherwise specified)		Limits Min	Max	Unit
Reference input	V_{REF}	$V_{KA} = V_{REF}$ see figure 3	$T_A = -55°C, +125°C$	2.42	2.57	V
			$T_A = +25°C$	2.44	2.55	
Cathode voltage	V_{KA10}	$V_{KA10} = V_{KA}$ $R_2 = 3.33\ k\Omega$, see figure 4		8.00	12.00	V
Cathode voltage	V_{KA36}	$V_{KA36} = V_{KA}$ $R_2 = 746\Omega$, see figure 4		31.00	36.00	V
Ratio of change in V_{REF} to change in V_{KA}	$\frac{V_R}{V_{K(1)}}$	$V_{REF} = V_{R2} - V_{R1}$ $V_{KA} = V_{KA10} - V_{R1}$ $R_2 = 3.33\ k\Omega$, see figure 4			-2.70	mV/V
Ratio of change in V_{REF} to change in V_{KA}	$\frac{V_R}{V_{K(2)}}$	$V_{REF} = V_{R3} - V_{R1}$ $V_{KA} = V_{KA36} - V_{R1}$ $R_2 = 746\Omega$, see figure 4			-2.00	mV/V
Reference input current	I_{REF}	$I_R = I_{REF}$ see figure 4	$T_A = +25°C$	-0.1	4.00	μA
			$T_A = -55°C, +125°C$	-0.1	7.00	μA
Minimum cathode current for regulation	I_{MIN}	$V_{KA} = V_{REF}$, $I_K = 1\ mA$ $R_2 = \infty$, see figure 3		2.40	2.60	V
Off-state cathode	I_{OFF}	$V_{KA} = 36\ V$, $V_{REF} = 0\ V$ see figure 5		-0.1	1.00	μA
Input impedance	Z_{KA}	$V_{KA} = V_{REF}$, $I_K = 1.0\ mA$ to 100 mA, see figure 3			0.50	Ω
Noise	N_O	$I_K = 10\ mA$ $B_W = 0.1\ Hz$ to 10 Hz see figure 6, $T_A = +25°C$			20.00	μVp-p

Table 3 Electrical Parameter Limits

DEVICE 1

TEST 1	2.4678 V	VREF1 AT 25 DEG C
TEST 2	9.8170 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.099 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.6788 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3864 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.7589 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4662 V	IMIN AT 25 DEG C
TEST 8	0.0149 UA	IOFF AT 25 DEG C
TEST 17	0.0003 OHMS	DYNAMIC IMPEDANCE
TEST 9	3.8042 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.0022 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4610 V	IMIN AT -55 DEG C
TEST 12	0.0370 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	9.3060 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.3330 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4347 V	IMIN AT 125 DEG C
TEST 16	0.1721 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

Table 4 Sample Test Data

DEVICE 2

TEST 1	2.4823 V	VREF AT 25 DEG C
TEST 2	9.8756 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.299 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.7552 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3662 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.7590 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4796 V	IMIN AT 25 DEG C
TEST 8	0.0158 UA	IOFF AT 25 DEG C
TEST 17	0.0004 OHMS	DYNAMIC IMPEDANCE
TEST 9	0.7830 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.0936 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.7491 V	IMIN AT -55 DEG C
TEST 12	0.1122 UA	IOFF AT -55 DEG C
TEST 18	0.0003 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	17.2195 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.2721 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4390 V	IMIN AT 125 DEG C
TEST 16	0.1674 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 3

TEST 1	2.4780 V	VREF1 AT 25 DEG C
TEST 2	9.8574 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.232 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.8119 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3139 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.6981 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4751 V	IMIN AT 25 DEG C
TEST 8	0.0121 UA	IOFF AT 25 DEG C
TEST 17	0.0003 OHMS	DYNAMIC IMPEDANCE
TEST 9	6.8483 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.1240 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4690 V	IMIN AT -55 DEG C
TEST 12	0.1278 UA	IOFF AT -55 DEG C
TEST 18	0.0003 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	13.5450 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.2113 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4415 V	IMIN AT 125 DEG C
TEST 16	0.1987 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 4

TEST 1	2.4742 V	VREF1 AT 25 DEG C
TEST 2	9.8445 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.186 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.7200 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3851 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.6373 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4718 V	IMIN AT 25 DEG C
TEST 8	0.0169 UA	IOFF AT 25 DEG C
TEST 17	0.0004 OHMS	DYNAMIC IMPEDANCE
TEST 9	4.8704 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	1.9110 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4665 V	IMIN AT -55 DEG C
TEST 12	0.1559 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	11.2619 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.4546 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4415 V	IMIN AT 125 DEG C
TEST 16	0.2077 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 5

TEST 1	2.4726 V	VREF1 AT 25 DEG C
TEST 2	9.8360 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.164 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.6692 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3942 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.7284 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4697 V	IMIN AT 25 DEG C
TEST 8	0.0155 UA	IOFF AT 25 DEG C
TEST 17	0.0004 OHMS	DYNAMIC IMPEDANCE
TEST 9	5.9347 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.2152 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4639 V	IMIN AT -55 DEG C
TEST 12	0.0964 UA	IOFF AT -55 DEG C
TEST 18	0.0003 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	11.5881 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.3330 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4339 V	IMIN AT 125 DEG C
TEST 16	0.2055 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 6

TEST 1	2.4762 V	VREF1 AT 25 DEG C
TEST 2	9.8526 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.225 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.7640 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3057 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.6373 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4742 V	IMIN AT 25 DEG C
TEST 8	0.0143 UA	IOFF AT 25 DEG C
TEST 17	0.0003 OHMS	DYNAMIC IMPEDANCE
TEST 9	6.3915 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.0328 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4671 V	IMIN AT -55 DEG C
TEST 12	0.0686 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	8.3704 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.3330 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4237 V	IMIN AT 125 DEG C
TEST 16	0.2198 UA	IOFF AT 125 DEG C
TEST 19	0.0008 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 7

TEST 1	2.4748 V	VREF1 AT 25 DEG C
TEST 2	9.8463 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.201 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.7267 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3229 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.7590 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4729 V	IMIN AT 25 DEG C
TEST 8	0.0184 UA	IOFF AT 25 DEG C
TEST 17	0.0003 OHMS	DYNAMIC IMPEDANCE
TEST 9	7.1526 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.1239 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4652 V	IMIN AT -55 DEG C
TEST 12	0.1374 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	5.9357 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.3025 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4382 V	IMIN AT 125 DEG C
TEST 16	0.1944 UA	IOFF AT 125 DEG C
TEST 19	0.0007 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 8

TEST 1	2.4809 V	VREF1 AT 25 DEG C
TEST 2	9.8721 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.287 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.6868 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.4180 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.7590 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4787 V	IMIN AT 25 DEG C
TEST 8	0.0146 UA	IOFF AT 25 DEG C
TEST 17	0.0004 OHMS	DYNAMIC IMPEDANCE
TEST 9	7.0229 MV	CHANGE IN VREF FORM -55 TO 25 DEG C
TEST 10	2.1240 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4705 V	IMIN AT -55 DEG C
TEST 12	0.3223 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	11.5891 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.6676 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4528 V	IMIN AT 125 DEG C
TEST 16	0.2017 UA	IOFF AT 125 DEG C
TEST 19	0.0005 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 9

TEST 1	2.4889 V	VREF1 AT 25 DEG C
TEST 2	9.9014 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.393 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.7656 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.4036 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.7590 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4864 V	IMIN AT 25 DEG C
TEST 8	0.0154 UA	IOFF AT 25 DEG C
TEST 17	0.0004 OHMS	DYNAMIC IMPEDANCE
TEST 9	5.3492 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.2153 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4803 V	IMIN AT -55 DEG C
TEST 12	0.0401 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	13.2627 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.3025 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4501 V	IMIN AT 125 DEG C
TEST 16	0.1672 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

DEVICE 10

TEST 1	2.4762 V	VREF1 AT 25 DEG C
TEST 2	9.8494 V	CATHODE VOLTAGE R2=3.33K OHMS
TEST 3	35.202 V	CATHODE VOLTAGE R2=746 OHMS
TEST 4	-0.8297 MV	CHG VREF/CHG VKA R2=3.33K OHMS
TEST 5	-0.3469 MV	CHG VREF/CHG VKA R2=746 OHMS
TEST 6	1.4243 UA	REF INPUT CURRENT AT 25 DEG C
TEST 7	2.4733 V	IMIN AT 25 DEG C
TEST 8	0.0167 UA	IOFF AT 25 DEG C
TEST 17	0.0004 OHMS	DYNAMIC IMPEDANCE
TEST 9	7.9136 MV	CHANGE IN VREF FROM -55 TO 25 DEG C
TEST 10	2.1239 UA	REF INPUT CURRENT AT -55 DEG C
TEST 11	2.4652 V	IMIN AT -55 DEG C
TEST 12	0.0968 UA	IOFF AT -55 DEG C
TEST 18	0.0004 OHMS	DYNAMIC IMPEDANCE AT -55 DEG C
TEST 13	12.7840 MV	CHANGE IN VREF FROM 25 TO 125 DEG C
TEST 14	1.2721 UA	REF INPUT CURRENT AT 125 DEG C
TEST 15	2.4373 V	IMIN AT 125 DEG C
TEST 16	0.2203 UA	IOFF AT 125 DEG C
TEST 19	0.0006 OHMS	DYNAMIC IMPEDANCE AT 125 DEG C

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